Design and Implementation of Triple Output Flyback Converter with Current Mode Control for Space Applications

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Abstract

This paper focuses on the design and implementation of triple output Flyback converter having built-in protection circuits to improve the reliability of the converter. The proposed converter is designed and realized with primary side current mode control technique using UC1846 PWM IC for faster response. The converter operates at a switching frequency of 200 kHz. Further, at the secondary side, Low Dropout Regulators (LDO) are employed for post regulation to achieve better, line, load and cross regulations. The experimental results of the converter producing triple outputs of 3.8 V/1 A, 5.6 V/0.5 A and 7.3 V/1 A from an input voltage that ranges from 26 V to 45 V and having an efficiency greater than 65% at full load are successfully obtained and hardware circuit implemented in this work.

Keywords. Flyback converter, post regulators, line and load regulations, current mode control.

1. INTRODUCTION

Switched Mode Power supplies have gained more popularity than the linear regulators because of its advantages like compact size, efficiency, reliability and ability to buck and boost the input voltage. Among the SMPS topologies, flyback topology is more commonly used for low to medium power application where isolation between input and output is required. Unlike Forward converters, Flyback converters does not require output filter for low current applications, which reduces the complexity, component count and space, which in turn greatly reduces the cost [1]. Hence flyback topology is selected here for multiple output requirement.

PWM technique is necessary to cope with the change in input voltage and output load. Hence to maintain a constant regulated output voltage, the duty of the main MOSFET is varied with constant switching frequency [2]. In this paper, UC1846 current mode controlled PWM IC is used [3]. Current mode control technique has advantages like faster transient response, simple compensation design and pulse to pulse current limiting ability. Multiple output converters with this control technique have poor load and cross regulation [4]. Hence to achieve tight line, load and cross regulation, Low Dropout Regulators (LDO) are used for post regulation at each output.

A wide range of operating temperature is necessary for any DC-DC converter to be able to use for space application for higher reliability purpose. Hence the proposed converter is

realised with components capable of operation at -55°C to 125°C range to achieve the requirement of -40 °C to +75 °C.

2. OPERATION AND DESIGN PROCEDURE

2.1. Converter Specification

- Input voltage range : 26 V to 45 V
- Switching Frequency : 200 kHz
- Output Parameters : +3.8 V/1 A, +5.6 V/0.5 A, +7.3 V/1 A
- Load regulation : ±1% (10% -100%load)
- Line regulation : ±1%
- Cross regulation : ±2%
- Ripple : <20mVpk-pk
- Operating Temperature : -40 °C to +75 °C
- Efficiency (100% load) : ≥65%

2.2. Converter Operation

The block diagram for the proposed 14W converter is illustrated in Figure 2.1 along with PWM controller, LDO regulators and protection circuits. The proposed converter operation is similar to that of a typical flyback converter. The flyback transformer acts as a choke i.e., when the MOSFET switch is ON, energy is stored in the primary winding of the power transformer and load is fed by the output capacitor. When the switch is OFF, the stored energy in the transformer is transferred to the secondary side and output capacitor replenish its charges and feeds the load.

The input voltage is applied through EMI filter which eliminates the common mode and differential mode noise. The start-up circuit provides the voltage to turn on the UC1846 PWM IC at the beginning and once the converter is completely turned on, bias voltage which is greater than start-up voltage will take over the start-up circuit. Here current sense resistor is used to measure the primary side current which is fed to UC1846 IC and is compared with the feedback error signal from the bias voltage feedback to generate PWM signals to drive the main MOSFET switch.

The switching frequency of the converter is accordingly adjusted by tuning the R_T and C_T of the PWM IC. The outputs at the secondary side are rectified and also filtered using Schottky diode and output capacitors respectively to generate the required RAW voltages. These RAW voltages are fed to respective post regulators, LDO's in order to obtain the regulated output of 3.8 V/1 A, 5.6 V/0.5 A and 7.3 V/1 A at the output stage. All protection circuits are of latch type and in case of any failure or abnormal conditions, shutdown pin of the PWM IC is latched to turn off the converter. Further, converter will not turn on unless the input is recycled.

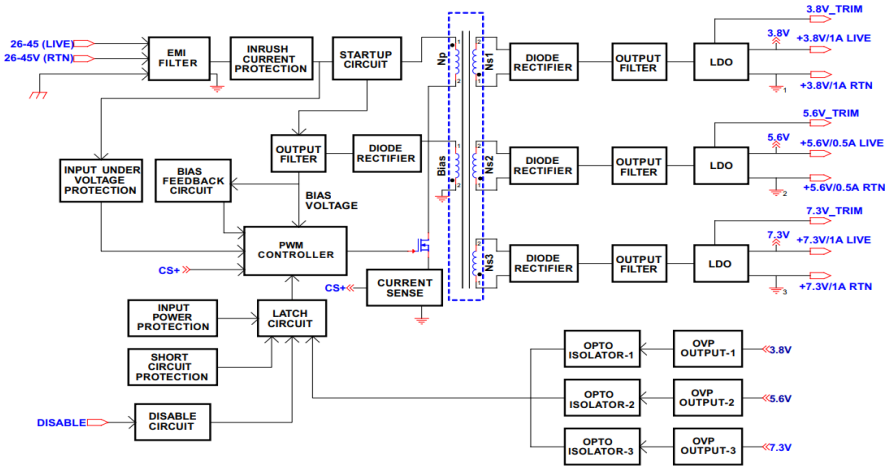


Figure 2.1. Block diagram of the proposed converter

3. DESIGN AND COMPONENT SELECTION

The design of the converter includes transformer design and core selection, controller design, MOSFET selection, output diode selection and also LDO regulator selection [5, 6].

Abbreviations:

$V_{in(min)}$	: Minimum input voltage	f_s	: Switching frequency
$V_{in(max)}$	: Maximum input voltage	E_{ff}	: Estimated efficiency
$V_{out(n)}$	: Output voltage for the nth output	K_w	: Window factor
V_D	: Diode voltage drop	J	: Current density
P_{in}	: Input Power	B_m	: Maximum flux density
P_{out}	: Output Power	A_p	: Area product of the core
D_{max}	: Maximum Duty	A_c	: Cross sectional area of the core
$I_{out(n)}$	: Output current for the nth output	A_W	: Window area of the core
$V_{ds(max)}$	: Maximum voltage stress of the MOSFET	N_p	: Number of turns for primary side
$T_{ratio(n)}$	: Transformer turns ratio for the nth output	$N_{s(n)}$	: Number of turns for the nth output
I_{pp}	: Input peak primary current	I_{srms}	: Secondary RMS current

I_{prms} : Primary RMS current

I_{dsp} : Maximum peak current of MOSFET

V_{RO} : Output voltage reflected to the primary

L_p : Transformer primary side inductance

3.1. Transformer design

The power transformer of the converter is designed using Area product (Ap) method [7].

Peak primary winding current is calculated by, $I_{PP} = \frac{2P_{out}}{D_{\max} V_{in(\min)}}$ (1)

Primary RMS current is calculated by, $I_{prms} = I_{pp}\sqrt{\frac{D_{\max}}{3}}$ (2)

Secondary RMS current is calculated by, $I_{srms(n)} = \frac{2}{\sqrt{3}}\left(\frac{I_{out(n)}}{\sqrt{1-D_{\max}}}\right)$ (3)

The primary inductance is calculated by, $L_p = \frac{(V_{in(\min)} D_{\max})^2}{2 * P_{in} f_s k_{rf}}$ (4)

Where, k_{rf} = Ripple factor = 0.3 (k_{rf} =1 for DCM operation and k_{rf} = 0.25 to 0.5 for CCM operation)

Area product formula is given by, $A_p = \frac{P_{out}\left(\frac{1}{E_{ff}}\sqrt{\frac{4D_{\max}\alpha}{3}} + \sqrt{\frac{4(1-D_{\max})\alpha}{3}}\right)}{K_w J B_m f_s}$ in mm^4 (5)

Where, Bm=0.18 $Tesla$, J= 4 A/mm^2, Kw=0.3, and α= 0.75

A core with area product greater than the calculated value is selected. Selected Toroidal core is: **CO55121-A2** with A_L value of 35nH /1000T.

Core area,A_C=19.2mm^2 and window area, A_W = 71.3mm^2

Area product for the selected core, $A_p = A_C A_W$ = 1369mm^4 (6)

Number of primary turns is given by, $N_p = \frac{L_p I_{PP}}{B_m A_C 10^{-6}}$ (7)

Turns ratio of each output is calculated by, $T_{ratio(n)} = \frac{(V_{out(n)} + V_D)(1-D_{\max})}{V_{in(\min)} D_{\max}}$ (8)

Number of secondary turns is calculated by, $N_{s(n)} = T_{ratio(n)} N_p$ (9)

3.2. MOSFET selection

The main MOSFET should be able to withstand the stress due to voltage spike by leakage inductance of the transformer, reflected voltage from the secondary and the maximum input voltage.

The reflected voltage on the MOSFET, $V_{RO} = \frac{D_{\max}}{(1-D_{\max})} V_{in(\min)}$ (10)

Maximum voltage stress on the MOSFET is calculated by the equation,

$$V_{ds(max)} = V_{in(\max)} + V_{RO} \quad (11)$$

The selected MOSFET is **BUY25CS12J** N-channel, V_{DS}= 250V, I_D= 12.4A, $R_{DS\ on}$= 0.13Ω

3.3. Output Diode selection

The voltage drop across the diode directly affects the efficiency of the converter. Schottky diodes are preferred as output diodes.

Reflected current is calculated by, $I_{s_{refelected(n)}} = \frac{(1-D_{\max})}{D_{\max}} * \frac{I_{dsp}}{\left(\frac{N_{s(n)}}{N_p}\right)}$ (12)

Reflected voltage is calculated by,

$$V_{s_{refelected(n)}} = \left(V_{out(n)} + V_D\right) + \left(\frac{N_{s(n)}}{N_p} V_{in(\max)}\right) \quad (13)$$

3.4. Current mode control

In conventional secondary side current mode control, the output voltage and current are measured and fed to respective error amplifiers. Output from the error amplifier is then applied to the PWM controller through an opto-coupler to generate PWM signal. This method has its drawbacks like complexity, increase in components count and space in PCB. Hence in this work, primary side current mode control is implemented where bias voltage from a separate bias winding provided in the converter which is used to power the PWM IC and other sub circuits, is also used as feedback to PWM controller [8, 9]. The primary current is measured indirectly by measuring the voltage drop across the current sense resistor which is in series with the source terminal of the main MOSFET switch.

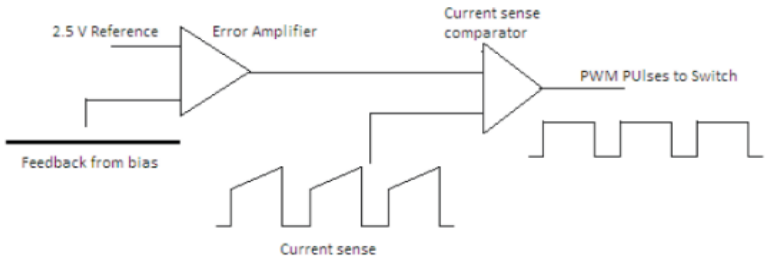


Figure 3.1. Current mode control scheme implemented in the converter

The sensed primary current produces ramp signal to the PWM controller which is then compared with the error amplifier output as demonstrated in Figure 3.1 to generate PWM signal for the required duty cycle to maintain constant output voltage. The UC1846 IC has

all the specific features having additional under voltage protection, current limiting and shutdown circuits.

3.5. LDO regulator

The Low Dropout Regulator comprises of an error amplifier and a series pass transistor (BJT/MOSFET). The main advantage of an LDO over a linear regulator is the varying dropout voltage. Drop out voltage is the minimum voltage difference between input and output to maintain regulation. Depending upon the change in input voltage and load, the error amplifier output varies the gate terminal of the series pass element. When the input voltage approaches the output voltage, error amplifier decreases/ increases the gate to source voltage V_{GS} for PMOS/NMOS series pass elements respectively, in order to reduce $R_{DS\ ON}$ to maintain regulation [10]. In this work, UC1834 IC is employed as post regulators along with external series pass device [11].

4. PROTECTION CIRCUITS

4.1. Under Voltage Protection (UVP)

The schematic for under voltage protection is presented in Figure 4.1. Resistor divider is used to set the UVP threshold voltage and is compared with the reference value. The threshold would always be higher than the reference value for 26V-45V input range. Once the input reduces below 22V, threshold is less than the reference and comparator output become high to latch the shutdown pin of PWM IC. The converter is turned on if input voltage is regained to 24V.

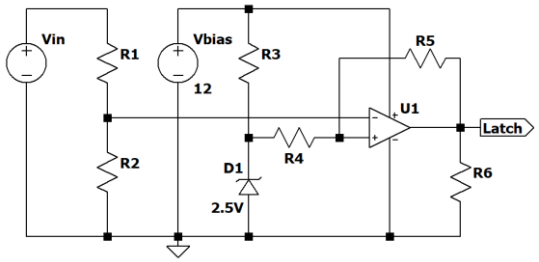


Figure 4.1 UVP circuit

4.2. Over Voltage Protection (OVP)

The schematic for output over voltage protection of one of the output terminals is presented in Figure 4.2. The comparator U1 continuously monitors the output voltage, when any of the three outputs increases beyond 125% of the nominal value, the output of U1 becomes high and through the opto-isolator drives the latch circuit to shut down the converter. Similarly, same OVP circuits are connected at each output terminals.

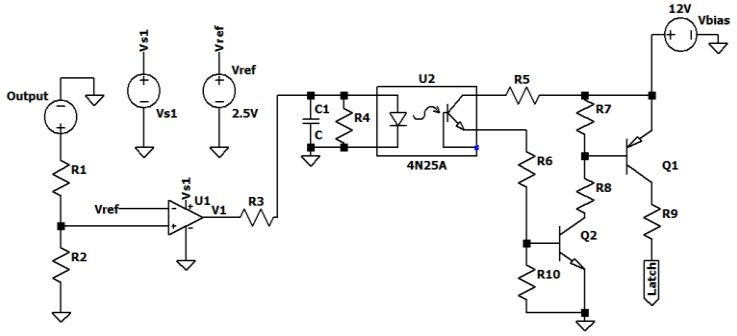


Figure 4.2 OVP circuit

5. HARDWARE IMPLEMENTATION AND RESULTS

The designed converter is effectively tested for an input voltage that ranges from 26V to 45V for different load conditions. Efficiency, line regulation, load regulation, cross regulation and ripple voltages are tabulated and presented in the following tables; TABLE I – V.

TABLE I. EFFICIENCY AT FULL LOAD

Input Voltage (V)	Input Current (A)	Output 1 (+3.8 V)	Output 2 (+5.6 V)	Output 3 (+7.3 V)	Efficiency (%)
26	0.7962	3.817	5.59	7.279	67.1
37	0.5685	3.817	5.59	7.28	66.04
45	0.4745	3.8174	5.591	7.28	65.06

Line regulation is calculated as follows,

$$\%\ Line\ regulation = \left(\frac{V_{out}\ at\ 26V - V_{out}\ at\ 45V}{V_{out}\ at\ 37V}\right) X\ 100 \quad (14)$$

TABLE II. LINE REGULTAION AT DIFFERENT LOADS

Load Condition	Line Regulation%		
	Output 1 (+3.8 V)	Output 2 (+5.6 V)	Output 3 (+7.3 V)
10% Load	0.00	0.00	0.00
50% Load	0.01	0.00	0.01
100% Load	0.01	0.02	0.01

Load regulation is calculated as follows,

$$\%\ Load\ regulation = \left(\frac{V_{out}\ at\ 10\%\ load - V_{out}\ at\ 100\%\ load}{V_{out}\ at\ 100\%\ load}\right) X\ 100 \quad (15)$$

TABLE III. LOAD REGULTAION FROM 10% LOAD TO 100% LOAD

Input Voltage (V)	Load Regulation%		
	Output 1 (+3.8 V)	Output 2 (+5.6 V)	Output 3 (+7.3 V)
26	0.50	0.34	0.48
37	0.49	0.34	0.46
45	0.48	0.32	0.46

Cross regulation is measured by keeping the measuring output at full load and other outputs at 10% load.

$$\%\ Cross\ regulation = \left(\frac{Measured\ output\ at\ 100\%\ load\ with\ remaining\ outputs\ at\ 10\%\ load - Measured\ output\ at\ 100\%\ load\ with\ remaining\ outputs\ at\ 100\%\ load}{Measured\ output\ at\ 100\%\ load\ with\ remaining\ outputs\ at\ 10\%\ load}\right) X\ 100 \quad (16)$$

TABLE IV. CROSS REGULATION AT DIFFERENT VOLTAGE

Input Voltage (V)	Cross Regulation%		
	Output 1 (+3.8 V)	Output 2 (+5.6 V)	Output 3 (+7.3 V)
26	0.02	0.02	0.01
37	0.01	0.02	0.01
45	0.01	0.02	-0.01

TABLE V. RIPPLE VOLTAGE AT FULL LOAD

Input Voltage (V)	Ripple voltage (mV)		
	Output 1 (+3.8 V)	Output 2 (+5.6 V)	Output 3 (+7.3 V)
26	3.20	4.20	5.20
37	3.60	3.60	4.20
45	3.80	4.20	6.00

Hardware setup for the designed converter is illustrated in Figure 5.1. The gate and drain voltages of the MOSFET is presented in Figures 5.2 and ripple voltages at 37V input with full load is presented in Figures 5.3. It is observed from the Figure 5.3 that Output voltage ripple value at different output terminals is within the specifications of the converter at 37V with full load.

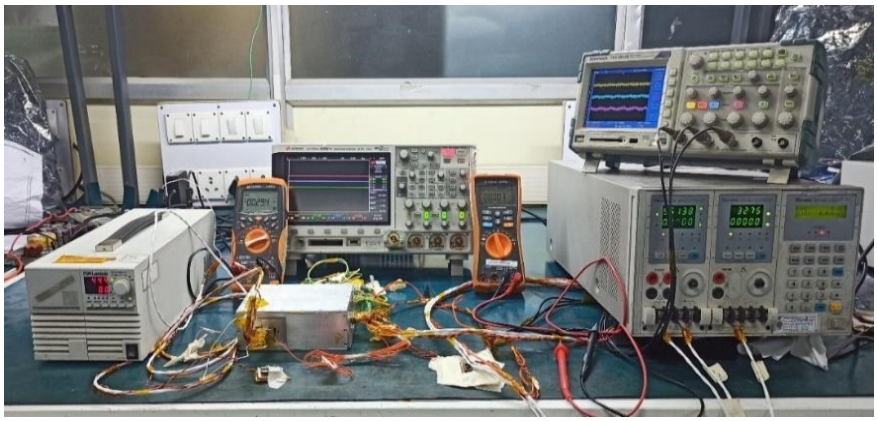


Figure 5.1. Hardware setup for the Converter with electronic load

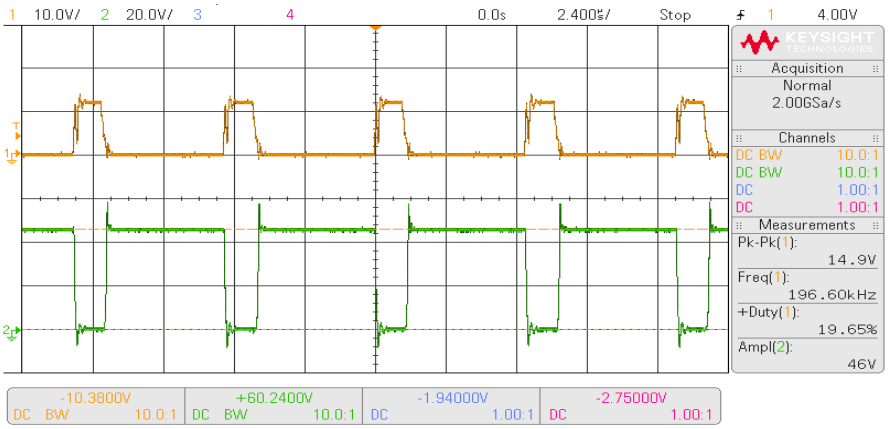
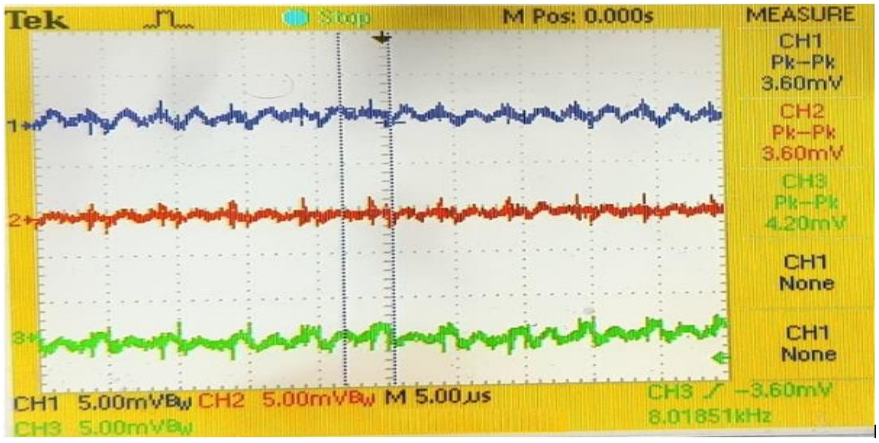


Figure 5.2. V_{GS} and V_{DS} at 37V with full load



Output 1 Output 2 Output 3

Figure 5.3. Output voltage ripple at 37V with full load

6. CONCLUSION

The triple output Flyback converter having primary side current mode control with post regulators is designed, analysed, implemented and tested for wide input voltage that ranges from 26V to 45V for all the load conditions. The converter is tested for extreme conditions: -40 °C to +75 °C temperature range. Further, designed value of the efficiency for the converter is effectively obtained around 65% at full load. The line, load and cross regulation results are presented and are found within the required specifications.

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