5

Reliability

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5.1 Mixed-mode Stress Tests

5.1.1 Introduction to Hot-Carrier Degradation under MM Stress

An important reliability concern in SiGe HBTs is related to long-term degradation (*stress* or *aging*) effects induced by hot carriers (HCs). While in MOSFETs HC mechanisms produce a degradation of drain current and transconductance, as well as a threshold voltage shift [Tya15], in bipolar transistors the HC damage is mainly related to the creation of Si dangling bonds acting as trap states at the semiconductor–insulator interfaces. Interface traps induced during device operation lead to an increased Shockley–Read–Hall (SRH) recombination and hence to an excess non-ideal base current component. Differently from MOSFETs, the collector current remains unaffected, and therefore it can in principle be stated that HC degradation is less critical in bipolar transistors, including the SiGe HBT technology; however, it still entails a number of undesirable consequences, such as current gain reduction (due to the base current growth), noise figure increase, shift of the bias point outside of the functional range, as well as increased power consumption in power amplifiers [Ven00, Cre04, Che09]. Such effects have been traditionally studied under reverse base–emitter stress conditions, where HCs are created by large electric fields across the base–emitter junction (see the early papers [Bur88, Gog00] and the more recent [Sas14a, Sas14b,

Fis15]); this stress test was indeed considered as appropriate for assessing device reliability in BiCMOS operation [Bur88].

Another stress technique has been subsequently proposed and quickly accepted in the literature, which is more representative of device degradation in practical mixed-signal and RF circuit applications; in this technique, referred to as *mixed mode* (MM) [Zha02], the device under test (DUT) is usually operated in common–base (CB) configuration while being simultaneously subjected to large emitter current density ($J_{\mathrm{E,stress}}$) and collector–base voltage ($V_{\mathrm{CB,stress}}$) [the corresponding V_{CE} being higher than the open-base breakdown voltage (BV_{CEO})] [Zhu05, Dio08, Cha15]. Although this biasing condition may seem too severe, the instantaneous operating point of a transistor (e.g., in oscillators and in noise/power amplifiers) can reach either high voltage or high current under large-signal operating mode, thereby gradually increasing HC-triggered damage [Che09, Fis08, Gre09, Fis15]. The high – and continuously applied – stress conditions $J_{\mathrm{E,stress}}$ and $V_{\mathrm{CB,stress}}$ are also denoted as *accelerating factors*, since they give rise to significant MM stress degradation in a relatively short time. Under MM stress tests, the trap creation process involves the following steps [Moe12]:

- the large electric field across the base–collector space-charge region (SCR) first creates primary HCs, and then additional (secondary, tertiary, and so on, depending upon $V_{\mathrm{CB,stress}}$) HCs by impact ionization (II);
- a fraction of the generated HCs can be directed toward the emitter–base oxide spacer (used to separate the Si emitter from the extrinsic base region) or the shallow trench (ST) oxide edge. Along these paths, they lose some energy due to collisions;
- if the HCs reach the oxide interfaces with an energy higher than 1.5 eV, then damage is produced in the form of dissociation of passivated Si–H bonds [Tya15, Tya16]. The damage spectrum depends on the accelerating factors $J_{\mathrm{E,stress}}$ and $V_{\mathrm{CB,stress}}$ for multiple reasons: first, they determine the II rate, but also the device temperature (high temperatures can have a beneficial impact in terms of damage recovery); moreover, they can trigger high-current (Kirk effect) or high-voltage (*pinch-in* effect) phenomena [Che07]. The trap creation at the emitter–base spacer (attributed to hot holes [Van06, Kam17b]) can be monitored by measuring the forward $V_{\mathrm{CB}} = 0$ V Gummel plot, where an SRH-induced growth in the low-V_{BE} base current is observed; the reverse $V_{\mathrm{EB}} = 0$ V Gummel plot is instead used to measure the damage due to HCs hitting the ST interface, since it causes an increase in the reverse-mode base current [Zha02, Zhu05, Che07, Moe12, Cha15].

5.1.2 Long-term MM Stress Characterization on IHP Devices

Mixed mode stress has been investigated in a recent exhaustive work [Fis15], where – differently from previous papers – *long-term* stress tests were performed, plainly showing a decrease in the degradation rate at long times. Moreover, an accurate investigation is presented, which includes the effect of: (i) the accelerating factors $J_{\mathrm{E,stress}}$ and $V_{\mathrm{CB,stress}}$, (ii) stress temperature, (iii) thermal recovery, and (iv) compact modeling of stress-induced base current components. The results of [Fis15] reported here refer to a packaged single-emitter SiGe:C NPN HBT fabricated by IHP, with effective emitter area[1] $A_{\mathrm{E}} = W_{\mathrm{E}} \times L_{\mathrm{E}} = 0.16\ \mu\mathrm{m} \times 0.52\ \mu\mathrm{m}$, W_{E} and L_{E} being the effective emitter width and length, respectively, featuring peak f_{T} of 250 GHz at $J_{\mathrm{C}} = 18\ \mathrm{mA}/\mu\mathrm{m}^2$, peak f_{MAX} equal to 300 GHz, $BV_{\mathrm{CEO}} = 1.7$ V, $BV_{\mathrm{CBO}} = 5$ V, and mounted in a CB configuration.[2]

The procedure can be described as follows. First, a Gummel plot is measured at $V_{\mathrm{CB}} = 0$ V, the HBT being still *fresh* (i.e., stress-unaffected). Then the stress bias (high $J_{\mathrm{E,stress}}$ and $V_{\mathrm{CB,stress}}$) is applied, and the evolution of the collector and base currents with stress (aging) time are monitored by measuring non-stressing $V_{\mathrm{CB}} = 0$ V Gummel plots at chosen time instants and recording their values at $V_{\mathrm{BE}} = 0.7$ V. Figure 5.1 shows the CB output

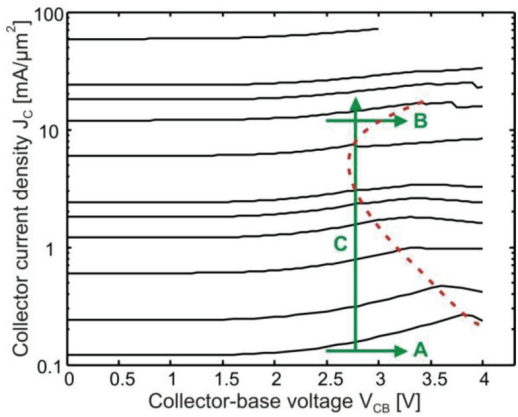

Figure 5.1 CB output characteristics of the DUT manufactured by IHP; also shown are the *pinch-in* locus (red dashed line) and the stress paths **A**, **B**, **C**.

[1] The effective emitter area is the area of the interface between Si emitter and SiGe base, which defines the vertical current flow.

[2] The analysis obviously requires the availability of a number of identical HBTs, one for each stress test to be performed.

characteristics of the DUT; also reported are the locus of *pinch-in* occurrence, which represents the limit of the CB safe operating area (SOA), and the stress conditions: in case **A**, identical transistors are biased with a low $J_{\mathrm{E,stress}}$ (=0.12 mA/μm^2) and different $V_{\mathrm{CB,stress}}$; in experiment **B**, other identical transistors are biased with a high $J_{\mathrm{E,stress}}$ = 12 mA/μm^2 (not far away from the current density at peak f_{T}) and different $V_{\mathrm{CB,stress}}$; in case **C**, $V_{\mathrm{CB,stress}}$ is kept constant at 2.75 V, and different $J_{\mathrm{E,stress}}$ are applied to identical transistors.

The first measurement campaign was conducted by forcing the transistor backside to a temperature T_{B} = 300 K through a thermochuck. In Figure 5.2,

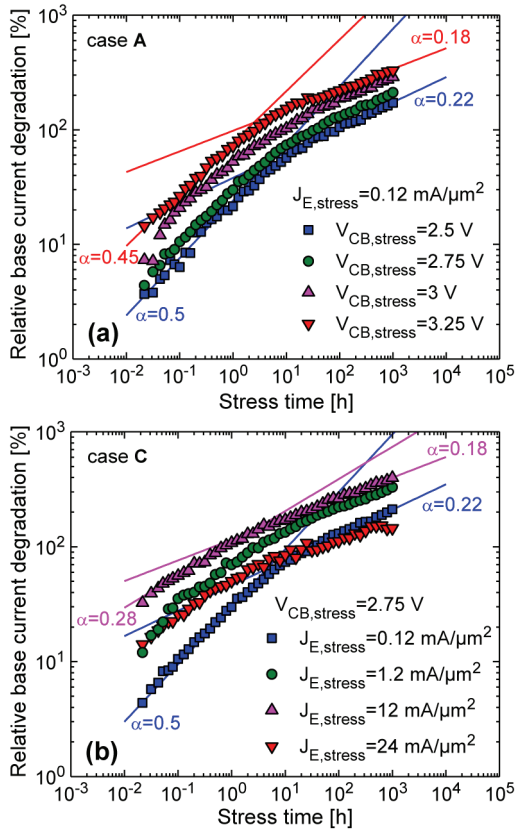

Figure 5.2 Relative base current degradation of the IHP HBT(s) as a function of stress time (a) for $J_{\mathrm{E,stress}}$ = 0.12 mA/μm^2 and various $V_{\mathrm{CB,stress}}$ (series **A**), and (b) for $V_{\mathrm{CB,stress}}$ = 2.75 V and various $J_{\mathrm{E,stress}}$ (series **C**). Also shown is extraction of exponent α at short and long stress times for selected cases.

the relative base current degradation $100 \cdot (I_{\mathrm{Bstress}} - I_{\mathrm{Bfresh}})/I_{\mathrm{Bfresh}}$ due to the enhanced recombination is shown for cases **A** and **C** at different values of $V_{\mathrm{CB,stress}}$ (**A**) and $J_{\mathrm{E,stress}}$ (**C**); it is found that the damage increases with stress time following a power law dependence ($\sim t_{\mathrm{stress}}^{\alpha}$). For short stress times (within a few hours), exponent α is around 0.5 for low/medium currents (consistent with [Che09]); on the other hand, it is found that the degradation rate decreases for longer stress times, where α approaches about 0.2. This is important in terms of device lifetime prediction (e.g., [Pan06]): if data are extrapolated from short-time experiments, the effect of degradation within a, e.g., 10-year timeframe would be largely overestimated. It must be remarked that the measured damage evolution does *not* indicate a trend to saturation within a 1,000-h-long stress time. From Figure 5.2(b) it can also be noted that the damage first increases with stress current, then reaches a maximum and declines at high currents (24 mA/μm^2). This "hump" behavior has also been observed in [Che07] and can be attributed to the higher temperature induced by self-heating (SH): when the temperature exceeds $\sim$350 K, damage indeed reduces as a result of (i) enhanced trap passivation, which starts dominating over trap creation, and (ii) increased carrier scattering, which reduces the number of highly energetic carriers reaching the interface. Moreover, the time exponent α is seen to lower at high currents [Fis13, Fis16]. Although not reported in the figures, this SH-induced reduction in degradation is also observed at high $V_{\mathrm{CB,stress}}$ for case **B**.

In order to investigate trap passivation occurring at high temperature, thermal annealing experiments were carried out. A high temperature of the base–emitter junction T_{j} (about 543 K)[3] was reached by increasing T_{B} to 398 K and raising the dissipated power (P_{D}) via the application of $V_{\mathrm{CB,anneal}}$ = 1.5 V and $J_{\mathrm{E,anneal}}$ = 30 mA/μm^2. Figure 5.3 illustrates the relative base current reduction $100 \cdot (I_{\mathrm{Banneal}} - I_{\mathrm{Bstress}})/I_{\mathrm{Bstress}}$ against anneal time for the previously stressed DUTs (series **A** in Figure 5.1). The main findings are: (i) the thermal annealing is more effective in transistors that underwent a heavier stress and (ii) significant current gain recovery is observed, independently of the stress load.

5.1.3 Medium-term MM Stress Characterization on IFX Devices

On-wafer medium-term MM stress tests were performed at University of Naples on single-emitter SiGe:C NPN BEC HBTs manufactured

[3]This value was assessed by a preliminary extraction of the thermal resistance.

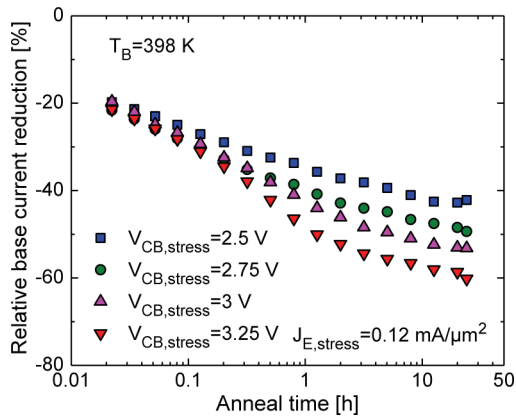

Figure 5.3 Relative base current reduction vs. anneal time obtained by applying T_{B} = 398 K, $V_{\mathrm{CB,anneal}}$ = 1.5 V, and $J_{\mathrm{E,anneal}}$ = 30 mA/μm^2 to IHP HBTs previously stressed with the bias conditions of Figure 5.2(a) (also reported in the legend). The monitoring of the base current was performed *in situ*, i.e., at T_{B} = 398 K for V_{BE} = 0.6 V and V_{CB} = 0 V.

by Infineon Technologies (hereinafter denoted as IFX) [Chev11]. The experiments were conducted on a device with effective emitter area[4] $A_{\mathrm{E}} = W_{\mathrm{E}} \times L_{\mathrm{E}} = 0.13 \times 2.73$ μm^2, exhibiting a peak f_{T} of 240 GHz, a peak f_{MAX} of 380 GHz at V_{CB} = 0.5 V, BV_{CEO} = 1.5 V, BV_{CBO} = 5.5 V,[5] and mounted in a CB configuration. Similar to the procedure in [Fis15], the stress experiments were conducted by applying high $J_{\mathrm{E,stress}}$ and $V_{\mathrm{CB,stress}}$ to the DUT, and monitoring the collector and base currents as a function of stress time through measurements of forward V_{CB} = 0 V Gummel plots at chosen stress times. A first investigation was carried out by considering different values of $J_{\mathrm{E,stress}}$ (namely, 1.4, 7, and 14 mA/μm^2) for the same $V_{\mathrm{CB,stress}}$ = 2 V. The relative base current degradation evaluated for V_{BE} = 0.7 V in the V_{CB} = 0 V Gummel plots is illustrated in Figure 5.4; it can be observed that (i) after 10^4 s the damage is still confined below 100% for all cases due to the low $V_{\mathrm{CB,stress}}$ applied, and (ii) the highest $J_{\mathrm{E,stress}}$ leads to a reduced degradation induced by the high temperature, as will be discussed in the following.

Another analysis was conducted by applying the lowest $J_{\mathrm{E,stress}}$ (=1.4 mA/μm^2) and three $V_{\mathrm{CB,stress}}$ values, namely, 2, 2.5, and 2.75 V.

[4]Further details on the technological definition of effective emitter area for IFX HBTs can be found in [dAl14].

[5]The transistor belongs to set #3 defined in 5.4.1; again, various identical devices were available, one for each stress test.

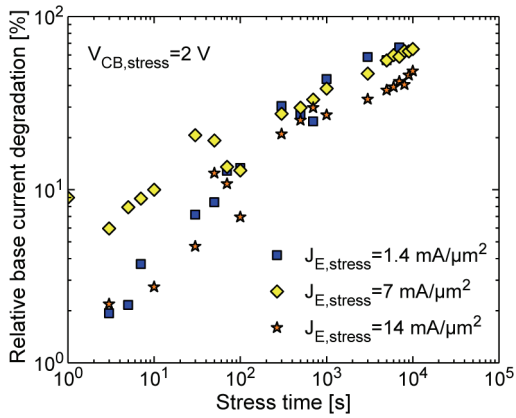

Figure 5.4 Relative base current degradation of the IFX device(s) vs. stress time for $V_{\mathrm{CB,stress}}$ = 2 V and various $J_{\mathrm{E,stress}}$.

Figure 5.5, showing the relative base current degradation at V_{BE} = 0.7 V, evidences that the damage increases with $V_{\mathrm{CB,stress}}$ due to the higher electric field in the base–collector depletion region, which in turn gives rise to a higher number of HCs with an energy higher than 1.5 eV impacting on the interface of the emitter–base oxide spacer and thus creating traps. It is found that the damage exceeds 100% for long times (10^4 s) for $V_{\mathrm{CB,stress}}$ = 2.5 V and even for very short times (300 s) for $V_{\mathrm{CB,stress}}$ = 2.75 V. Consistently with other works, Figure 5.6 witnesses that a power law ($\mathrm{t}_{\mathrm{stress}}^{\alpha}$) well describes

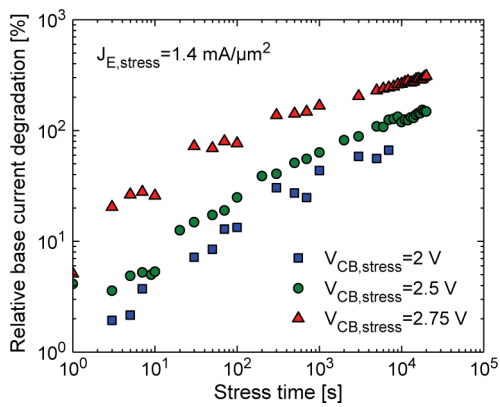

Figure 5.5 Relative base current degradation of the IFX DUT(s) against stress time for $J_{\mathrm{E,stress}}$ = 1.4 mA/μm^2 and various $V_{\mathrm{CB,stress}}$.

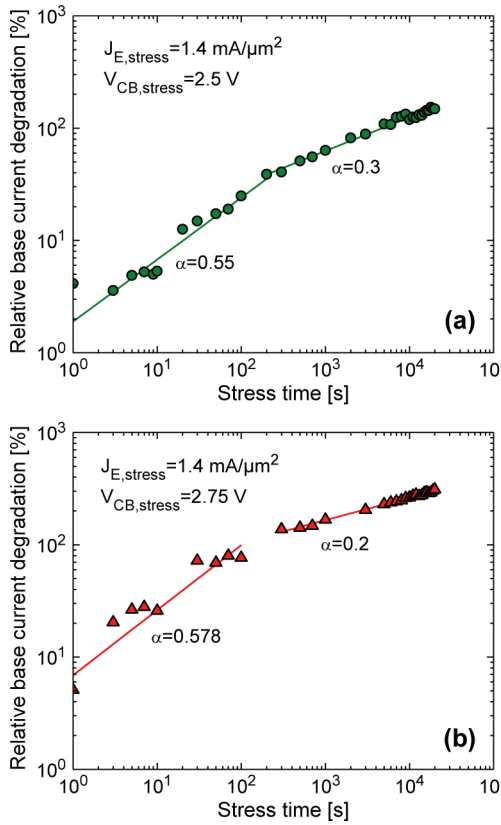

Figure 5.6 Relative base current degradation of the IFX device(s) as a function of stress time for $J_{\mathrm{E,stress}}$ = 1.4 mA/μm^2 and (a) $V_{\mathrm{CB,stress}}$ = 2.5 V, (b) $V_{\mathrm{CB,stress}}$ = 2.75 V. Also shown is the extraction of exponent α at short and medium times.

the evolution of the base current degradation, provided that a different α is considered for short (high α) and medium (low α) stress times.

Following the approach presented in [Van06], an analysis was carried out to gain an in-depth insight into the device behavior under MM stress conditions. In particular, a fresh DUT identical to the stressed ones was measured by sweeping V_{CB} for various assigned J_{E}s. After a straightforward data processing based on the technique in [Lu89, Zan93] and on the knowledge of the thermal resistance R_{TH} = 7,000 K/W (determined according to the method in the section "Experimental R_{TH} Extraction"), it was possible to obtain the $J_{\mathrm{AV}} - J_{\mathrm{E}}$ (J_{AV} being the avalanche current density) and $T_{\mathrm{j}} - J_{\mathrm{E}}$ curves shown in Figure 5.7. It can be inferred that at low J_{E} the avalanche

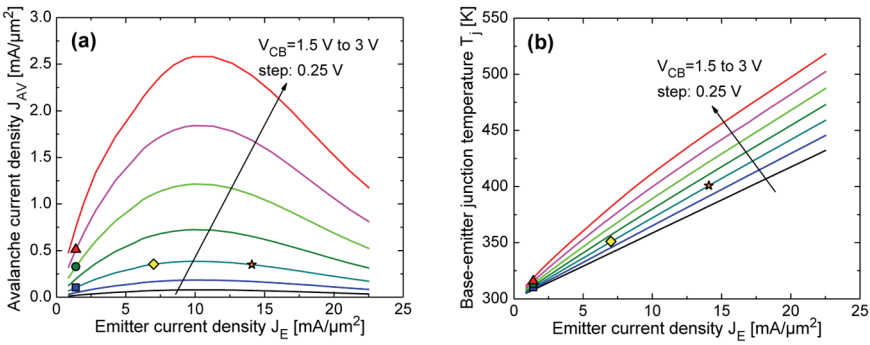

Figure 5.7 (a) Avalanche current density J_{AV} and (b) base–emitter junction temperature T_{j} as a function of emitter current density J_{E} for various V_{CB}s. Also shown are the conditions corresponding to the stress tests reported in Figures 5.4 and 5.5 (the same symbols were used for the sake of clarity).

current J_{AV} grows with J_{E} as a result of the increased II related to the higher number of electrons traveling to the base–collector SCR; conversely, J_{AV} decreases at high J_{E} due to the concurrent mitigating impact of high-injection (HI) and SH effects. Also identified in Figure 5.7 are the J_{AV}s and T_{j}s corresponding to the MM stress conditions related to Figures 5.4 and 5.5. The main findings are in agreement with the conclusions in [Van06] and can be summarized as follows:

- although the stress test with applied $J_{\mathrm{E,stress}}$ = 14 mA/μm^2 (star) shares the same J_{AV} (≈0.3 mA/μm^2) and V_{CB} (=2 V) as the test with $J_{\mathrm{E,stress}}$ = 7 mA/μm^2 (rhombus), in the first case the damage is lower due to the higher device temperature (400 K instead of 300 K, as shown in Figure 5.7(b));
- conversely, the tests carried out at the same current density $J_{\mathrm{E,stress}}$ = 1.4 mA/μm^2 and different V_{CB}s (square, circle, and triangle) share similar temperatures and different J_{AV}s (the avalanche current increases with V_{CB} due to the higher electric field in the base–collector SCR). As a result, the damage grows with increasing V_{CB}.

5.2 Long-term Stress Tests

The improved frequency performances of state-of-the-art SiGe HBTs have been achieved at the cost of significantly increased operating current densities and lower breakdown voltages [Sch17]. Thus, devices are often operated

closer and even beyond the border of the classical SOA; however, this can limit stable device operation due to reliability issues induced by the previously discussed HC degradation. In the following, some dedicated long-term stress tests are carried out to clearly identify the influence of biasing conditions along the SOA limit on the device reliability [Jac15].

5.2.1 Experimental Setup

The stress tests were conducted on devices biased in a common-emitter (CE) configuration under bias conditions close to the SOA border. Since these conditions are not *accelerating* like in conventional MM tests, a long stress time (up to 1,000 h) was required to observe an impact on the electrical characteristics. The transistors are single-emitter SiGe:C NPN CBEBC HBTs fabricated by IFX, with an effective emitter area of A_E = 0.13 × 9.93 μm^2 featuring a peak f_T/f_{MAX} equal to 240/380 GHz and a BV_{CEO}/BV_{CBO} of 1.5/5.5 V [Chev11, Böc15]. In order to observe and record the evolution of the base and collector currents during the tests, non-stressing forward (at V_{CB} = 0 V) and reverse (at V_{EB} = 0 V) Gummel plots were measured at fixed time instants during the 1,000 h-long experiments [Jac15]. Four stress bias conditions, referred to as P1, P2, P3, and P23, were applied at T_B = 300 K along the SOA boundary, as shown in Figure 5.8. The corresponding

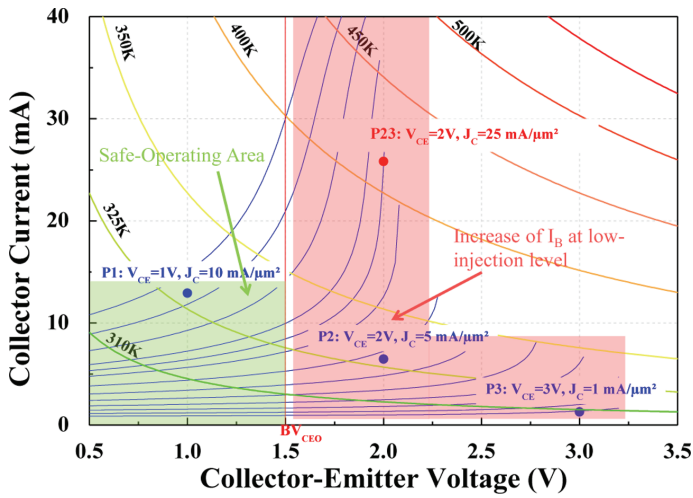

Figure 5.8 Output characteristics of the SiGe HBT under test simulated using HICUM/L2. Also represented are the examined bias conditions (P1, P2, P3, and P23).

voltage (V_{CE}), collector current (I_C), and current density (J_C), as well as the (average) temperature rise ΔT_j over the base–emitter junction (obtained from the thermal resistance R_{TH} = 2,850 K/W determined with the approach in [dAl14]) are summarized in Table 5.1. It must be remarked that P1 is defined below BV_{CEO}, whereas P2, P3, and P23 are beyond BV_{CEO}.

5.2.2 Long-term Degradation Test Results

For P1, P2, and P3, the tests were performed on six HBTs for each bias condition, (that is, 18 identical HBTs were measured). Figure 5.9 shows the forward V_{CB} = 0 V Gummel plots during the stress test at P1, P2, and P3, while Figure 5.10 illustrates the aging-induced I_B growth at V_{BE} = 0.713 V. The following considerations are in order.

- At P3, I_B increases regularly with stress time for low V_{BE}; at V_{BE} = 0.713 V, the variation is 120 nA after 1,000 h.
- At P2, I_B slightly increases for low V_{BE}; at V_{BE} = 0.713 V, the variation amounts to 80 nA after 1,000 h.
- At P1, no sizable degradation is monitored.

In conclusion, the higher V_{CE}, the more the low-injection I_B increases with stress time.

It must be remarked that a slight natural recovery is observed if the device stays *on the shelf* between two stress periods. This recovery is visible at 300 h in Figure 5.10 for the biasing conditions P2 and P3 (the devices were left unstressed for 24 h before the measurement of the Gummel plot).

Concerning P23, the forward V_{CB} = 0 V Gummel plots for each stress time are shown in Figure 5.11, which indicates that I_B increases at low V_{BE}, while remaining almost constant at high V_{BE}. The relative variation of the base current at V_{BE} = 0.65 V is shown in the inset, along with the variation measured at P2 for an identical HBT. The comparison highlights that I_B exhibits similar evolutions at P23 and P2 due to the same collector–emitter voltage (V_{CE} = 2 V), in spite of the four times higher J_C at P3.

Table 5.1 Stress bias conditions and corresponding junction temperatures

	P1	P2	P3	P23
V_{CE} [V]	1 ($<BV_{CEO}$)	2 ($>BV_{CEO}$)	3 ($>BV_{CEO}$)	2 ($>BV_{CEO}$)
I_C [mA]	12.9	6.45	1.29	32.27
J_C [mA/μm^2]	10	5	1	25
ΔT_j [K]	37	37	11	184

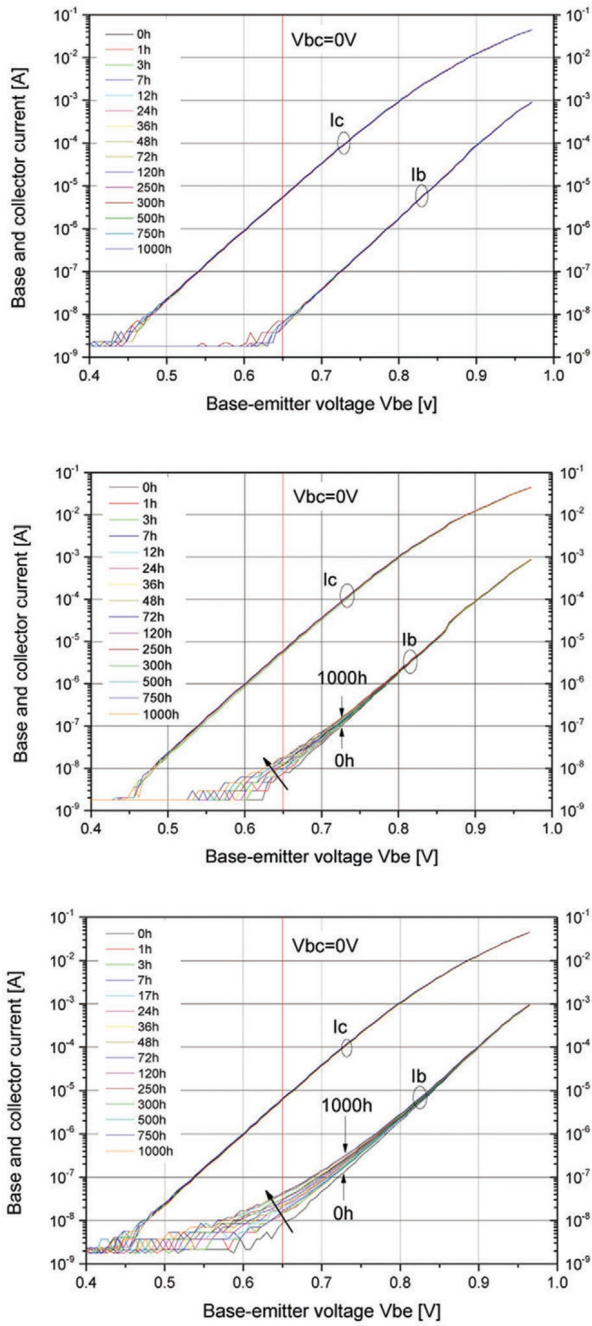

Figure 5.9 Monitoring forward Gummel plots for the DUT stressed at P1, P2, and P3.

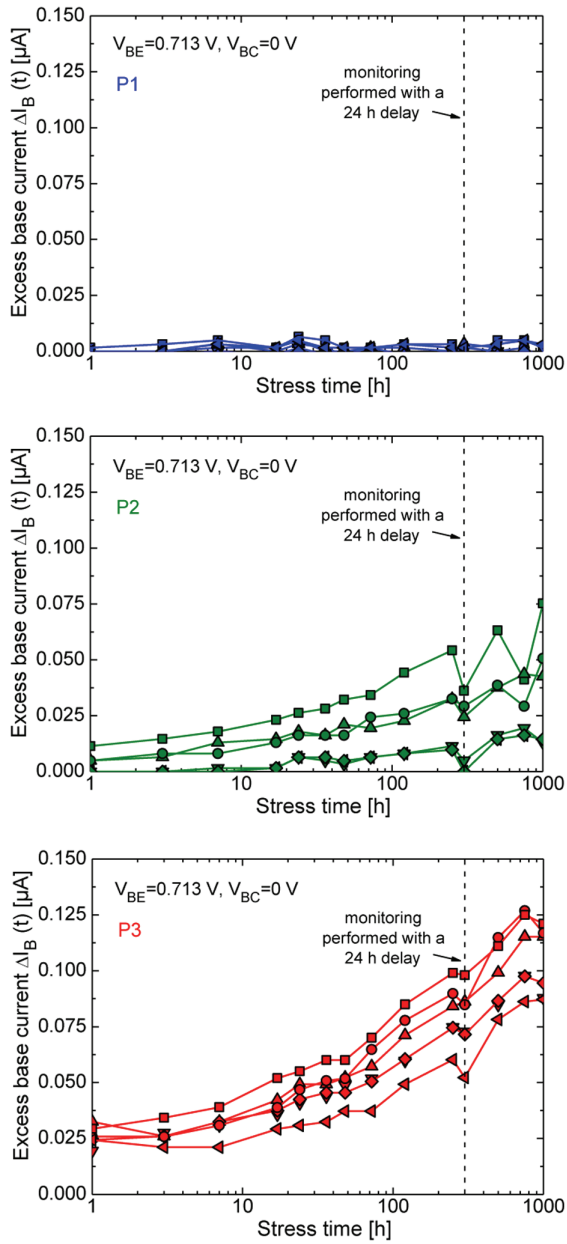

Figure 5.10 Evolution of the excess base current as a function of stress time for six identical HBTs tested at P1, six HBTs tested at P2, and six HBTs tested at P3.

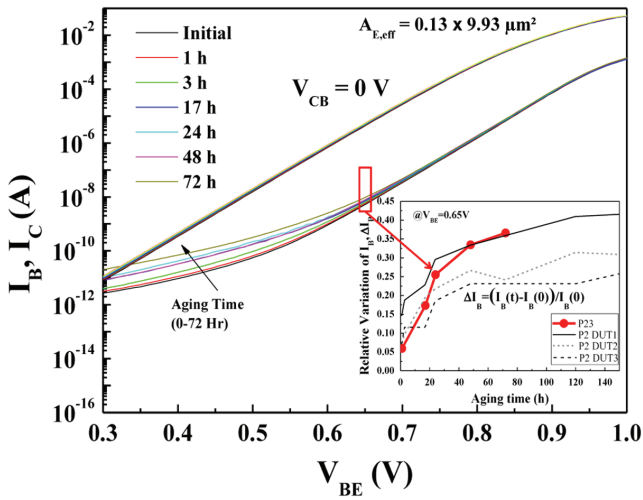

Figure 5.11 Evolution of the forward Gummel plot with stress (aging) time at P23. Shown in the inset is the relative variation of I_{B} at V_{BE} = 0.65 V.

The reverse V_{EB} = 0 V Gummel plots were also measured for all biasing conditions at chosen time instants during the stress tests. Since the DUTs have the emitter and substrate connected to the ground pad, the base voltage was fixed to 0 V to obtain V_{EB} = 0 V, and a negative collector voltage was swept from 0 V to –1 V to increase V_{BC}. Due to the forward biasing of the substrate–collector junction, a substrate current is added to the emitter current. It was found that the sum of the emitter and substrate currents remains almost constant regardless of the bias point, as can be inferred for the P23 case in Figure 5.12. Different behaviors were instead observed for the $I_{\mathrm{B}} - V_{\mathrm{BC}}$ curves: Figure 5.12 also witnesses that at P23 I_{B} tends to rapidly increase during the first few hours for $V_{\mathrm{BC}} < 0.6$ V, eventually saturating after 48 h (as shown in the inset), while remaining constant for $V_{\mathrm{BC}} > 0.6$ V. No significant degradation of the reverse Gummel plot was instead observed at P2 (despite the same V_{CE} as P23) and P3 [Jac15]. It is also worth noting that the distortion measured in the reverse V_{EB} = 0 V $I_{\mathrm{B}} - V_{\mathrm{BC}}$ plot for low V_{BC} at P23 resembles that of the forward V_{CB} = 0 V $I_{\mathrm{B}} - V_{\mathrm{BE}}$ plot at low V_{BE}.

The forward I_{B} increase observed at low V_{BE} at P2, P3, and P23 has been attributed to hot holes generated by II ($V_{\mathrm{CE}} > BV_{\mathrm{CEO}}$) at the base–collector SCR and then driven by the electric field to cross the base and hit the edge of the spacer with enough energy to create traps, as determined in

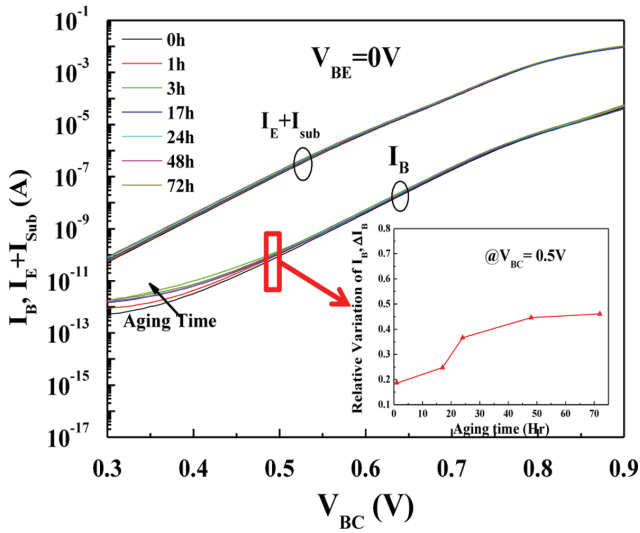

Figure 5.12 Evolution of the reverse Gummel plot with stress (aging) time at P23. Shown in the inset is the relative variation of I_{B} at V_{BC} = 0.5 V.

[Kam17b] with an advanced TCAD simulation strategy based on the solution of the Boltzmann Transport Equations for electrons and holes through the Spherical Harmonic Expansion approach (see Chapter 2). As clarified in the section "Introduction to hot-carrier degradation under MM Stress," the traps in turn lead to a non-ideal I_{B} growth via trap-assisted SRH recombination. The higher damage occurring at P3 is due to the higher electric field within the base–collector SCR, which implies a higher concentration of hot holes with enough energy to break the passivated Si–H bonds [Kam17b].

On the other hand, the damage at the ST–Si interface (witnessed by the distorted $I_{\mathrm{B}} - V_{\mathrm{BC}}$ plots) at the high-current P23 condition may be associated with both hot holes and hot electrons induced by II, as suggested in [Moe12].

The physical locations of the defects are illustrated in Figure 5.13 with the help of a cross section obtained from a TCAD simulation of the device structure. It is shown that the upper region of the ST–Si interface is more affected by hot holes, whereas the lower region is more affected by hot electrons.

Another numerical analysis was performed using Sentaurus TCAD by Synopsys [Syn] to obtain a deep insight into the degradation mechanism; the hydrodynamic model with optimized parameters reported in [Sas10] was activated. More specifically, simulations were performed to extract the

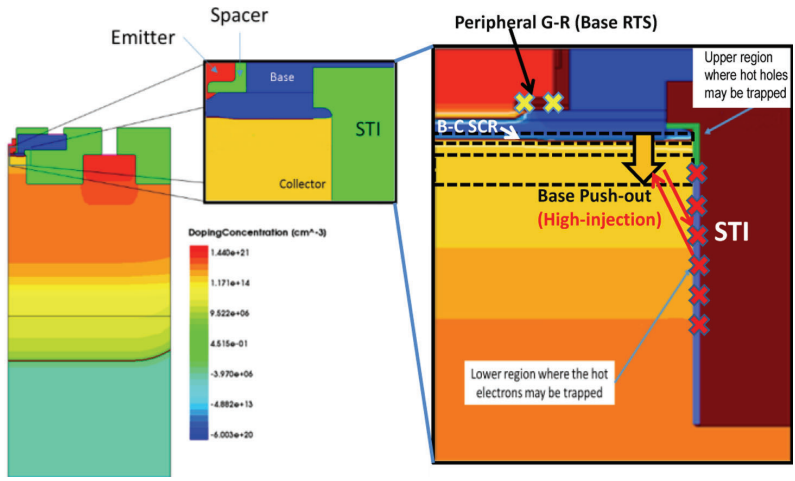

Figure 5.13 Physical origin of the base current degradation represented in a cross section within a TCAD environment.

evolution of the trap density N_t at the spacer interface (P2, P3, and P23) and ST–Si interface (only P23) as follows: for each time instant at which the non-stressing forward and reverse Gummel plots were measured and recorded, N_t (assumed to be at an assigned energy level E_t such as $E_t - E_V = 0.6$ eV, E_V being the valence band limit) was optimized so as to align the simulated plots with the experimental ones. Figure 5.14 reports the matching between measured and computed forward $V_{CB} = 0$ V Gummel plots at P3 after 7 and 750 h. Figure 5.15 illustrates the extracted N_t at the spacer interface as a function of stress time for P2 and P3 [Jac15].

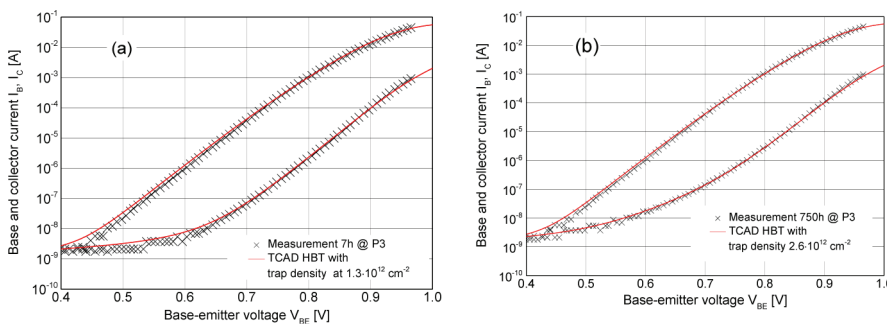

Figure 5.14 Forward Gummel plots at $V_{CB} = 0$ V at P3 after (a) 7 h and (b) 750 h of stress. Measurement results (symbols) are compared with the simulated (solid) counterparts.

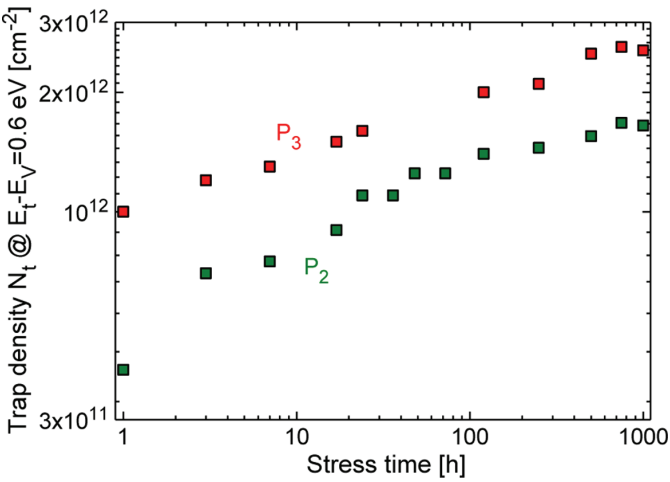

Figure 5.15 Trap density evolution along the interface of the emitter–base oxide spacer vs. stress time at P2 and P3.

5.2.3 Low-frequency Noise Characterization

Noise characterization can be considered as a diagnostic tool for analyzing quality and reliability of bipolar transistors [Vand94, Moh00]. Flicker noise is ubiquitous in almost every electronic device, although its origin is still deep in dispute. Unlike silicon BJTs, current HBTs are often affected by significant generation-recombination (G-R) noise (not so common in large-area devices) at low frequencies, mostly originated in the device external surface and periphery [Cos92, Tut95]. These noise sources may lead to presence of significant random telegraph signal (RTS) noise that can be observed in the time-domain noise signal.

Hereinafter, a comprehensive analysis of the RTS noise in IFX SiGe:C HBTs is presented, in which dominant G-R mechanisms are evidenced at low bias currents in smaller geometries, as confirmed by RTS noise measurements [Muk17]. In larger geometries the RTS noise is not so frequently observed. Eventually, extractions of RTS time constants and their evolution with bias are analyzed to get insight into the active G-R mechanisms. The weak evolution of the RTS noise amplitude with bias indicates that the noise sources are located in the base–emitter peripheral region. Consequently, distinct RTS is observed at the collector side that is activated at high current regimes. This indicates the activation of traps located in trench areas due to fixed imperfections.

The noise characterization setup includes a Keysight E5270B semiconductor parameter analyzer for DC biasing, an HP 35670A dynamic signal analyzer for the measurement of voltage noise spectral density, and a Femto DLPVA-100-F-S low-noise voltage amplifier, which has a variable gain up to 100 dB with a bandwidth of 100 kHz and an 1 TΩ input impedance. The measurements were performed at a gain of 40 dB. The entire on-wafer measurement system is connected through a GPIB interface and is controlled via the ICCAP software. The noise spectral densities of the transistors are measured in V^2/Hz (averaged over 20 spectra). The time-domain RTS noise voltage was measured using the dynamic signal analyzer. The system noise floor was determined to be 2×10^{-17} V^2/Hz. During the biasing, a very high source resistance (R_S) was considered due to the current source for the base biasing, and a 50 Ω resistance was used as load resistance (R_L). The values of transistor parameters β, r_π, R_E, and R_B were extracted from DC measurements. The RTS noise was measured on single-emitter SiGe:C NPN HBTs fabricated by IFX (see the sections "Medium-term MM Stress Characterization on IFX Device" and "Experimental Setup") with various terminal configurations and effective emitter areas, as summarized in Table 5.2. In order to eliminate process variation, the noise was measured on several devices (five to eight) of the same geometry from different dies.

The forward Gummel plot for HBT #3 is shown in Figure 5.16, which depicts the bias range of the noise measurements.

Figure 5.17 shows the base voltage noise spectral density (S_{V_B}) for transistor #1 at V_{BE} = 0.7 V and V_{CE} = 1 V. It can be clearly observed that two distinct G-R mechanisms (referred to as GR1 and GR2) are active. For all the investigated geometries, high G-R noise was observed in the low-frequency noise spectra at lower bias. These G-R noise mechanisms were particularly visible in smaller geometries. The corresponding RTS are shown in the two insets. Interestingly, it is found that one RTS (GR2)

Table 5.2 Details of the DUTs for RTS noise measurements

N°	Configuration	A_E(=$W_E \times L_E$) [μm^2]
1	BEC	0.13 × 2.71
2	BEBC	0.13 × 4.91
3	CBEBC	0.11 × 9.93
4	BEBC	0.17 × 9.91
5	BEBC	0.25 × 9.91
6	BEBC	0.61 × 9.91
7	BEBC	1.61 × 9.91

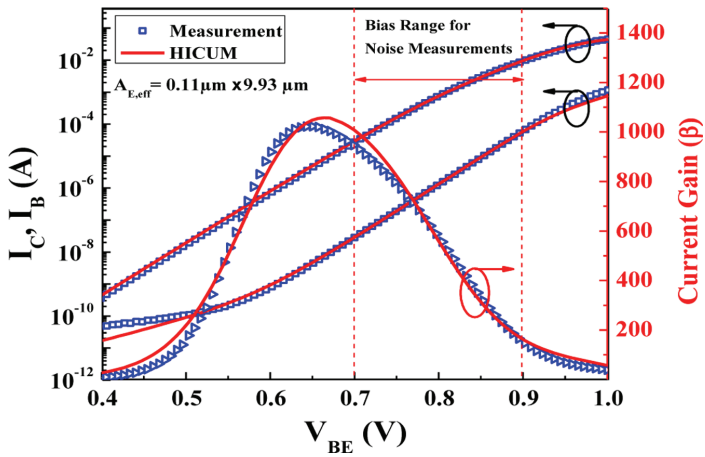

Figure 5.16 Forward Gummel plot showing the bias range for noise measurements.

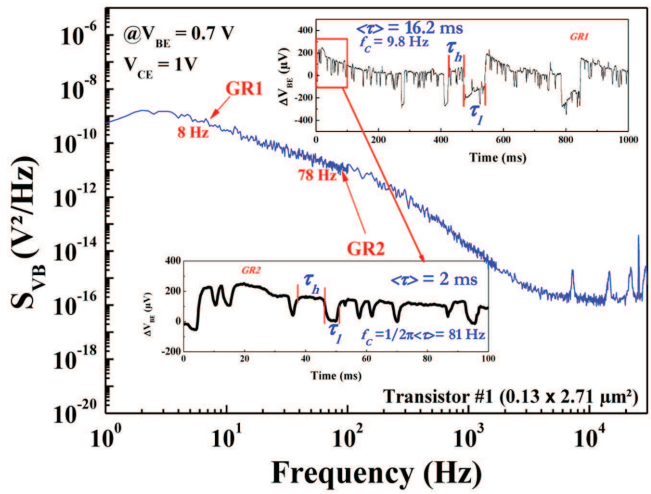

Figure 5.17 S_{V_B} showing different G-R mechanisms and their corresponding RTS in time domain for transistor #1.

is superimposed on the other (GR1). The measured S_{V_B} shows GR1 at a frequency of 8 Hz while the corresponding RTS measurement reveals an average time constant $<\tau>$ of 16.2 ms, equivalent to a G-R cutoff frequency (f_C) of 9.8 Hz (since $\tau = 1/2\pi f_C$). This confirms the existence of GR1. The other RTS (GR2) can be observed in the 0–100 ms range of the time-domain signal superimposed on the principal RTS (GR1) having a smaller

time constant of 2 ms (f_C = 81 Hz) that corresponds to the GR2 at 78 Hz. In [Pas04], the observations are quite similar for SiGe HBTs, where a G-R is observed only at low bias and in a frequency range below 100 Hz for smaller devices; it was illustrated from time analysis that this G-R component is related to RTS noise. In our results, the bias dependence shows a weak evolution of the RTS amplitudes. This indicates that such a G-R mechanism is not located in SCRs, and possibly originates at base–emitter periphery [vHa02]. Similar G-Rs were observed in base current noise spectra in earlier stages of this work [Muk16a, Muk16b].

Figures 5.18 and 5.19 illustrate the S_{VB} and the corresponding RTS at different bias conditions for the smallest (transistor #1) and largest (#7) geometries, respectively. Significant G-R contributions are clearly observed with large RTS time constants in #1, whereas #7 does not show significant G-R at low frequencies. For example, at V_{BE} = 0.725 V, transistor #1 exhibits significant GR1 (at 10 Hz) and GR2 components (around 40 Hz), which correspond to time constants of 15 ms and 3 ms (superimposed RTS) in the RTS spectra, respectively. As the bias increases, the RTS time constants become smaller, indicating a faster response from the traps, and at higher bias, such as 0.9 V, the G-R mechanisms completely disappear leading to absence of any RTS in the time-domain noise response. Transistor #7 does not show dominant G-R contribution: a minor G-R contribution can be seen around 105 Hz (time constant of 1.5 ms) that is observed in the RTS at V_{BE} = 0.7 V.

Evidently, the existence of significant RTS noise in smaller geometries is well accepted [Pas04]. In our case, the RTS corresponds to the existence of GR1 in the noise spectral density at low frequency, which we have identified as a contribution due to emitter periphery.

Figure 5.20(a) shows the base RTS noise response of transistor #4 at different bias conditions. Figure 5.20(b) witnesses that the RTS time constants at both the low (τ_1) and high (τ_h) states scale with 1/exp(qV_{BE}/kT), except for the highest V_{BE} where the devices are entering the medium/high injection regime. The capture rate of carriers inversely depends on the available carrier density in the trap position, which can increase with bias. However, a small electric field decrease in the SCR due to a higher V_{BE} is not sufficient to turn into such a rapid roll-off in the characteristic time [vHa02]. This indicates that there must be an additional bias dependence on the trapping and de-trapping mechanisms. In [vHa02], the authors explained their results by tunneling of electrons from the neutral regions across the SCR into traps located in the spacer oxide near the periphery. As V_{BE} increases, the tunneling distance decreases due to reduced SCR width, resulting into faster trap response and therefore reduced RTS time constants (Figure 5.20(b)).

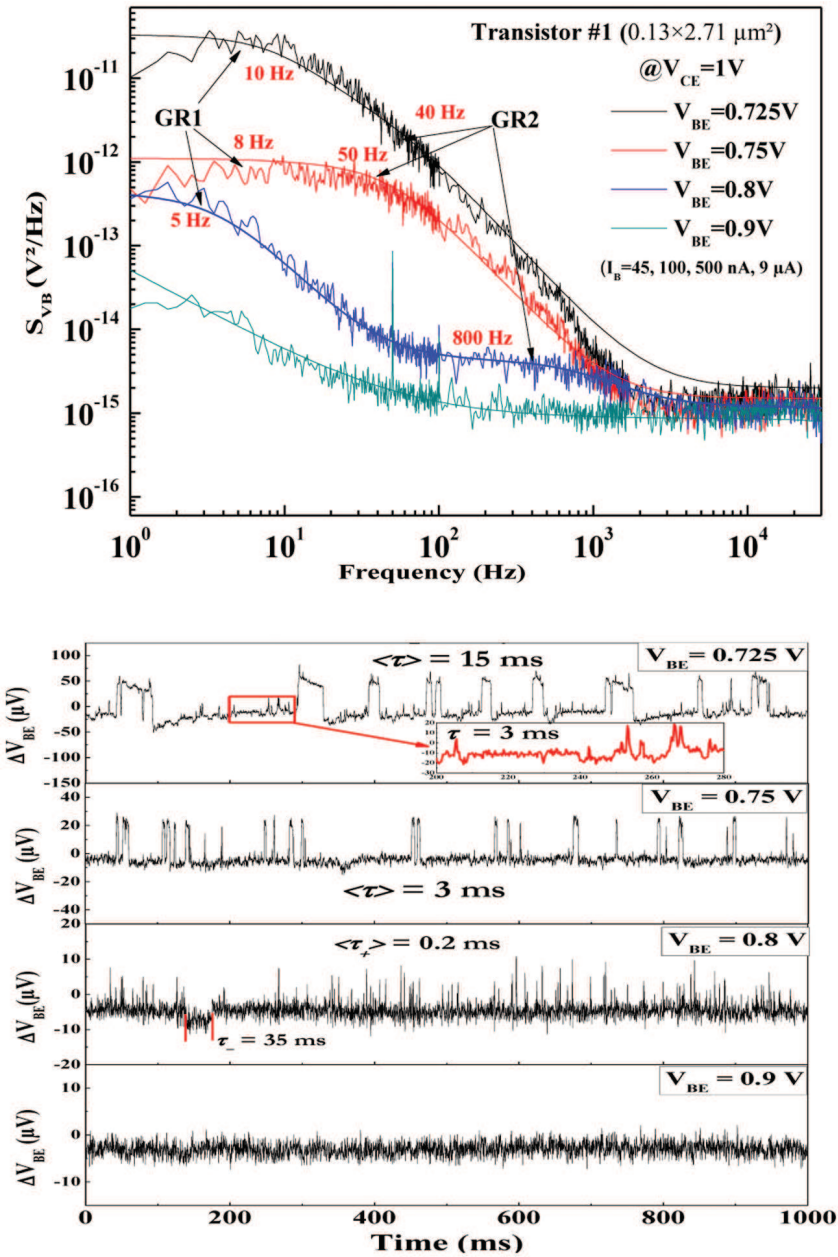

Figure 5.18 S_{V_B} showing different G-R mechanisms at different bias (V_{BE}) conditions and their corresponding RTS in time domain for transistor #1.

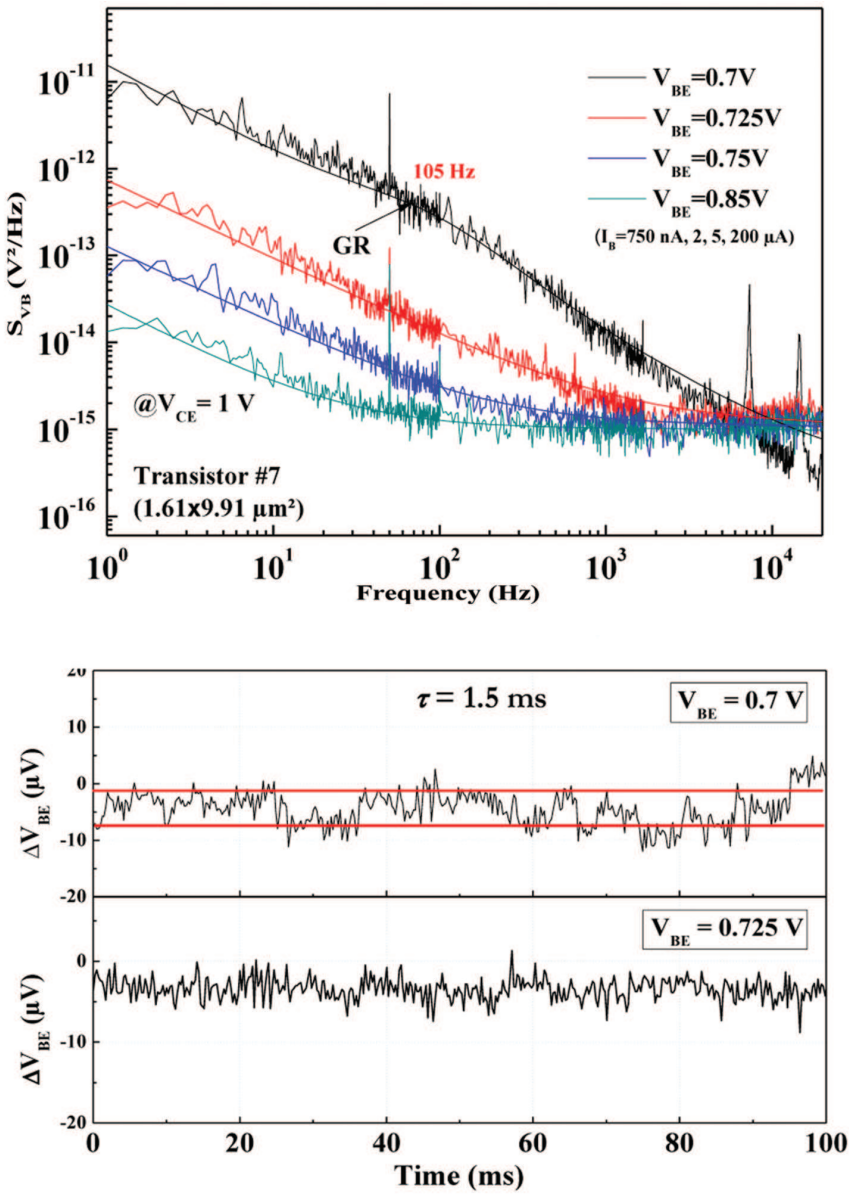

Figure 5.19 S_{V_B} showing different G-R mechanisms at different bias (V_{BE}) conditions and their corresponding RTS in time domain for transistor #7.

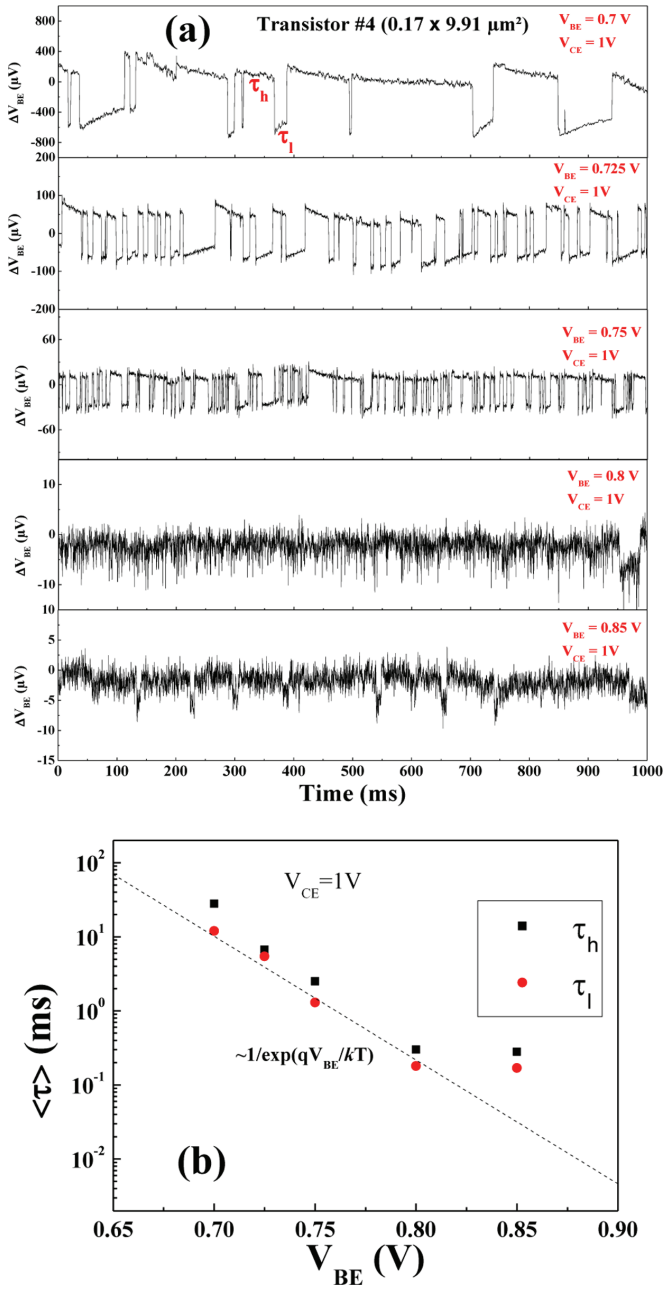

Figure 5.20 (a) Base RTS at different bias conditions, (b) corresponding time constants for the low and the high states as a function of bias (V_{BE}) for transistor #4.

Figure 5.21 shows the RTS noise current amplitude (ΔI_B) of the base noise for different geometries. A very weak bias current dependence ($\sim {I_B}^{0.1}$) is found for smaller transistors, and an almost insignificant dependence is observed for larger geometries. This further corroborates that the RTS noise sources at the base side are located in the emitter–base periphery regions. Also in [vHa02] it was stated that when ΔI_B scales with non-ideal base current component, these fluctuations often originate from noise sources in the spacer oxide at the emitter periphery. In our HBTs a large dispersion in $\Delta I_B/I_B$ ratios was observed (between 0.3% and 3%) from device to device. In larger devices the $\Delta I_B/I_B$ ratio has a relatively higher magnitude, yet this ratio inversely scales with I_B in all geometries. Different $\Delta I_B/I_B$ ratios indicate slightly different physical origins of traps in different geometries.

The bias dependence of the collector RTS is presented in Figure 5.22(a), which shows the RTS at different V_{CB}s for transistor #5. Figure 5.22(b) illustrates the extracted trap time constants as a function of the collector–base bias for two geometries (#4 and #5) at V_{BE} = 0.9 and 0.8 V, respectively. It is expected that the time constants of high and low states are higher in larger geometries at lower bias since the tunneling distance is higher. However, the characteristic times remain almost constant for higher V_{CB}s in both cases, and the steady-state value is reached faster in the case V_{BE} = 0.9 V (onset of high-current effects), whereas a sharp transition at lower V_{CB} is

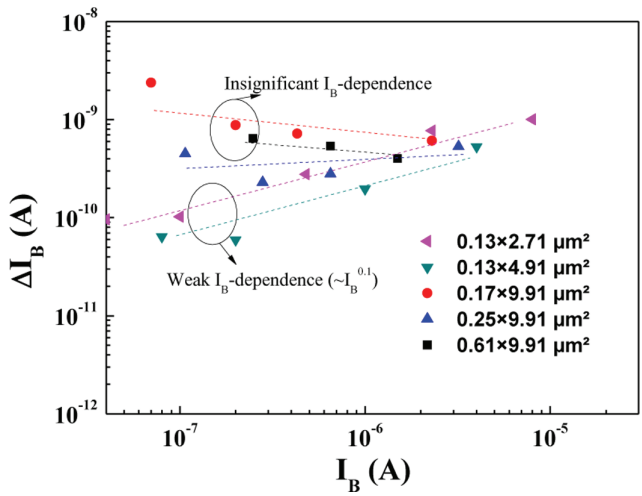

Figure 5.21 Base noise RTS amplitude (ΔI_B) as a function of bias (I_B) for different transistor geometries.

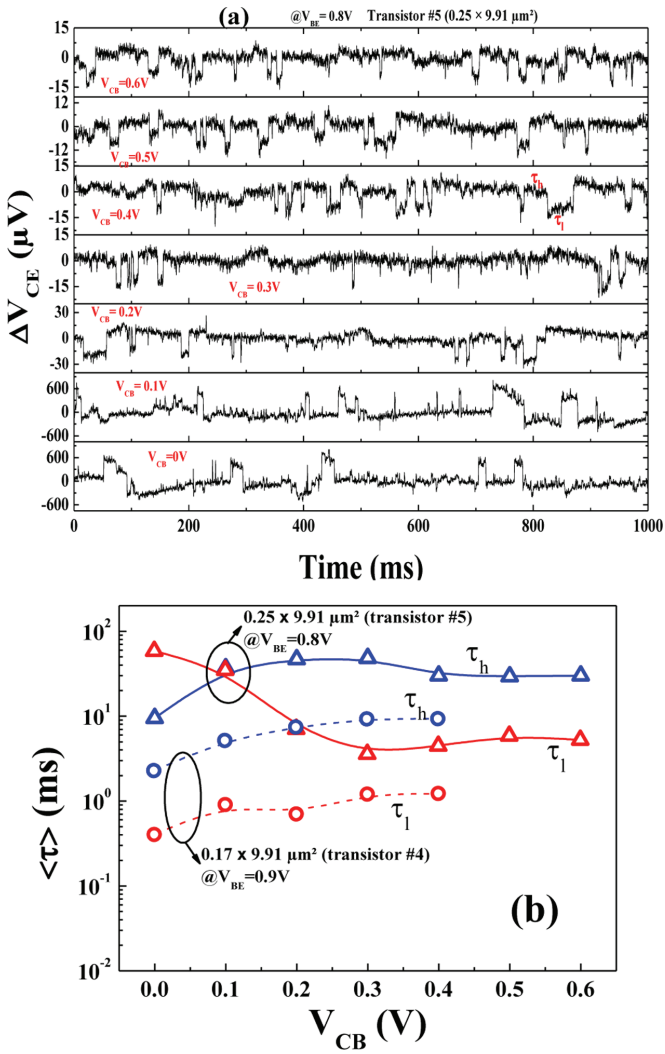

Figure 5.22 (a) Collector RTS at different bias conditions and (b) corresponding RTS time constants as a function of bias (V_{CB}) for transistors #4 and #5.

observed at V_{BE} = 0.8 V. The saturation of trap response at higher V_{CB} indicates that these RTS noise sources are possibly located at the top of the ST walls, and even if the base–collector SCR enlarges, the trap density at the trench sidewalls remains fixed. At V_{BE} = 0.8 V, a sharp transition is observed when the SCR is narrow (V_{CB} ∼0.1 V), and with the SCR spreading

the tunneling time constants change due to activation of new traps until it reaches saturation. Conversely, due to high-injection (V_{BE} ∼0.9 V) and base pushout effects, tunneling times remain constant since all the sidewall traps are already aligned within the SCR area.

In conclusion, this comprehensive analysis of the RTS noise in advanced SiGe:C HBTs demonstrates the evidence of dominant G-R mechanisms at low bias currents in smaller geometries, whereas in larger geometries the RTS noise is not observed. The bias dependence of the RTS reveals a weak evolution in the noise amplitude indicating that the noise sources are located in the base–emitter peripheral region. Distinct RTS is observed at the collector side also near high current regimes, which was attributed to activation of traps located in ST walls. This highlights the applicability of RTS noise characterization to probe these imperfections via non-destructive means.

5.3 Compact Modeling of Hot-Carrier Degradation

The technology selection for the fabrication of integrated circuits is mainly driven by both performance and reliability criteria; in particular, the lifetime is one of the most crucial factors. To evaluate lifetime, the aging behavior of a specific degradation effect can be studied with TCAD simulations focusing mostly on bias-temperature instability and HC injection in MOSFETs, and on MM degradation in bipolar transistors. TCAD simulations can provide some in-depth information on the physical mechanisms. However, these simulations are done at the expense of very long simulation times, thus making them unviable for circuit design. Hence, it is necessary to develop a more practical circuit simulation platform using electrical compact models at transistor level suited to efficiently capture the physics of the degradation through aging laws and subsequently reflect it at circuit level.

5.3.1 Empirical Equations by IHP

Based on the long-term stress results discussed in the section “Long-term Degradation Test Results,” IHP developed the following empirical equation for the base current degradation:

$$\Delta I_{\mathrm{B}} = C_{\mathrm{MM}} \cdot f\left(V_{\mathrm{CB,stress}}, J_{\mathrm{E,stress}}\right) \cdot \left(c_{\mathrm{JE}} \cdot t_{\mathrm{stress}}\right)^{\alpha(t_{\mathrm{stress}})} \tag{5.1}$$

where t_{stress} is the stress (aging) time and α is a time-dependent power factor [Fis15, Fis16]. By referring to the early stress stage ($t < 0.1$ h), this general dependence on the stress conditions was extracted [Fis15]:

$$f\left(V_{\mathrm{CB,stress}}, J_{\mathrm{E,stress}}\right) = \exp\left(\mu_0 V_{\mathrm{CB,stress}}\right) \cdot \left(\frac{1\ \mathrm{mA/\mu m^2}}{J_{\mathrm{E,stress}}} + \frac{J_{\mathrm{E,stress}}}{J_{\mathrm{Ehc}}}\right)^{-0.5} \tag{5.2}$$

where μ_0 = 1.5 V^{-1} and J_{Ehc} = 25 mA/$\mu\mathrm{m}^2$.

The long-term development of the logarithmic aging rate

$$\alpha_{\log} = d\left(\log \Delta I_{\mathrm{B}}\right) / d\left(\log t_{\mathrm{stress}}\right) \tag{5.3}$$

can be approximately fitted to the observed base current degradation by means of the power coefficient

$$\alpha\left(t_{\mathrm{stress}}, J_{\mathrm{En}}\right) = 0.2 + \frac{0.3}{\left(t_{\mathrm{stress}} + J_{\mathrm{En}}^{0.45}\right)^{0.18 \cdot J_{\mathrm{En}}^{0.4}}} \tag{5.4}$$

with pre-factor $c_{\mathrm{JE}} = J_{\mathrm{En}}^{-1}$ and $J_{\mathrm{En}} = J_{\mathrm{E,stress}}/J_{\mathrm{Emin}}$, i.e., the stress current density normalized to the minimum applied density J_{Emin} = 0.12 mA/$\mu\mathrm{m}^2$. This equation is rather complex because $J_{\mathrm{E,stress}}$ has enormous influence on the development of aging rate, as can be seen in Figure 5.23, where aging over a range of stress currents and up to 1,000 h has been successfully simulated by modifying the recombination current of an HBT compact model with the above equations.

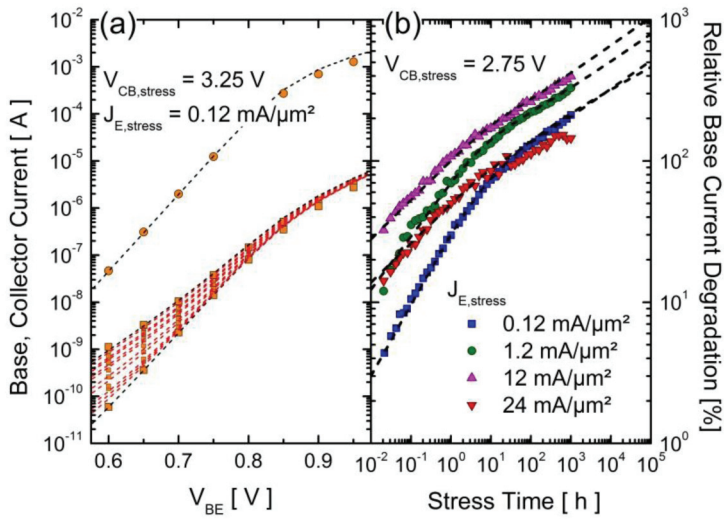

Figure 5.23 (a) Forward Gummel plots and (b) base current degradation of IHP HBTs simulated with an empirical aging function (dashed lines).

5.3.2 HICUM-based Model

Various compact models have been developed for mm-wave circuit applications. One of the most commonly used model for SiGe:C HBTs is referred to as HIgh CUrrent Model (HICUM) [Sch05, Sch10, Sch13], and is based on the General Integral Charge-Control Relation (GICCR) [Sch93]. The GICCR allows taking into account the relevant transport mechanisms through a physical-based approach; this is the reason why HICUM was chosen to implement the aging laws based on the experimental results presented in the section "Long-term Degradation Test Results."

As described before, the degradation (i.e., the base current growth at low V_{BE}) is due to an HC-induced increase in trap density over the interface of the emitter–base oxide spacer. In HICUM the base current in forward mode is subdivided into various components [Sch10], namely, the current I_{jBEi} injected into the intrinsic part of the emitter as a main component, and the peripheral current, in turn composed of the back-injection current across the emitter perimeter junction I_{jBEp} and the recombination current in the perimeter base–emitter SCR I_{REp}; I_{jBEp} and I_{REp} are given by:

$$I_{\mathrm{jBEp}} = I_{BEpS} \cdot \left[\exp\left(\frac{V_{\mathrm{BEjp}}}{m_{\mathrm{BEp}} V_{\mathrm{T}}} \right) - 1 \right] \tag{5.5}$$

$$I_{\mathrm{REp}} = I_{\mathrm{REpS}} \cdot \left[\exp\left(\frac{V_{\mathrm{BEjp}}}{m_{\mathrm{REp}} V_{\mathrm{T}}} \right) - 1 \right] \tag{5.6}$$

where V_{BEjp} is the peripheral internal (junction) base–emitter voltage, while the saturation currents I_{BEpS} and I_{REpS}, as well as the non-ideality factors m_{BEp} and m_{REp}, are model parameters. In [Gho10, Gho11], it was shown that a possible approach to simulate the I_{B} degradation in InP HBTs is to use I_{REp} given by Equation (5.6). More specifically, the I_{REpS} evolution is expected to follow the N_{t} evolution vs. t_{stress} (extracted as, e.g., in the section "Long-term Degradation Test Results"). In a simplified approach in which I_{REpS} is assumed to saturate for long stress times, the dependence of I_{REp} on time can be accounted for in HICUM through the following differential equation for I_{REpS}:

$$\frac{dI_{\mathrm{REpS}}}{dt} = ATSF \cdot (G - R \cdot I_{\mathrm{REpS}}) \tag{5.7}$$

where G is the generation rate and R (fitting parameter) the annihilation rate of traps, while ATSF is an Aging Time Scale Factor added to shorten the

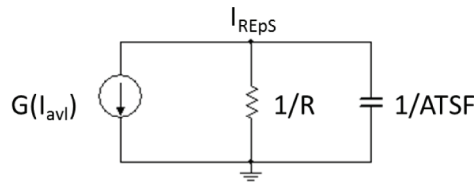

Figure 5.24 New transistor circuit used for aging law implementation in HICUM.

simulation time needed to have a perceptible stress effect to minutes (instead of tens of hours). The generation rate G depends on the bias conditions; in particular, it is an increasing function of the collector–base voltage (V_{CB}) due to the enhanced II current I_{AV} (accounted for in HICUM [Sch10]). The following linear relation was proposed in [Jac15] to include this dependence:

$$G = A \cdot I_{\mathrm{AV}} + G_0 \tag{5.8}$$

A and G_0 being fitting parameters. Equation (5.7) with (5.8) was implemented in the Verilog-A code of HICUM/L2 by including the additional circuit shown in Figure 5.24.

5.4 Thermal Effects

Thermal issues have become a serious concern in SiGe HBTs due to the concurrent impact of the following factors: (i) the shrinking of the intrinsic device has induced a growth in power density within the base–collector SCR for a given bias condition; (ii) the trench isolation – exploited to reduce parasitics, crosstalk, and increase f_{MAX} – limits the heat spreading since trenches are filled with materials suffering from low thermal conductivity [Rie05, dAl10, You11, Pet15]. This mechanism is even exacerbated by lateral scaling, which results in a horizontal reduction of the Si volume embraced by trenches; (iii) HBTs are operated at high current densities to boost the frequency performance, which entails a further increase in dissipated power density [Cre13]. Owing to these considerations, thermal effects can be viewed as an undesired, yet unavoidable, by-product of the technology evolution. Unfortunately, the enhanced heat generation (for a given dissipated power) and the reduction in heat removal have pushed the thermal resistances (R_{TH}) of SiGe HBTs into the thousands of K/W [ElR12, Has12, Sah12] and even beyond 10^4 K/W for small emitter windows, as evidenced by recent experimental campaigns conducted on transistors fabricated by STMicroelectronics

(hereinafter referred to as STM) [dAl10] and IFX [dAl14]. Thermal effects can lead to a severe distortion of the DC device characteristics (e.g., [LaS09]), and also degrade the low-frequency and high-frequency (since the DC bias is altered) behavior; besides the performance penalty, they may also affect the long-term reliability, and even trigger destructive instability phenomena. Consequently, care must be taken in assessing the impact of the thermal behavior in advanced technology nodes.

5.4.1 Experimental R_{TH} Extraction

Since the steady-state thermal behavior of a device is fully described by the thermal resistance (R_{TH}), a plethora of methods to experimentally extract this critical parameter in bipolar transistors have been developed. Among them, particular interest has been paid to approaches based on DC measurements, for which low effort and relatively cheap instrumentation are required. The most widespread method – presented in slightly different variants in the literature [Daw92, Pfo03, Rie05] – relies on the measurement (i) of the temperature-sensitive base–emitter voltage to employ its temperature coefficient as a *thermometer*, and (ii) of the base–emitter voltage as a function of collector–base voltage (or dissipated power) at an assigned emitter (collector) current. A sticking point of this technique is the thermometer calibration, which can be impacted by SH and thus entail a thermal resistance overestimation. A strategy to purify this procedure from SH has been proposed by Vanhoucke et al. [Van04]. Here an alternative to [Van04] is presented, which suggests a logarithmic law for the current dependence of the temperature coefficient of the internal (junction) base–emitter voltage V_{BEj} and can be explained as follows.

In the absence of HI and II effects, the collector current $\mathrm{I_C}$ of a SiGe HBT (which exhibits marginal Early effect) can be described by the simple model

$$I_{\mathrm{C}} = A_{\mathrm{E}} J_{S0} \exp\left[\frac{V_{\mathrm{BEj}} + \phi\left(I_{\mathrm{E}}\right)\Delta T_{\mathrm{j}}}{\eta V_{\mathrm{T0}}}\right] \tag{5.9}$$

where V_{BEj} is given by:

$$V_{\mathrm{BEj}} = V_{\mathrm{BE}} - R_{\mathrm{E}} I_{\mathrm{E}} - R_{\mathrm{B}} I_{\mathrm{B}} \tag{5.10}$$

R_{B}, R_{E} being the parasitic base and emitter resistances. In Equation (5.9), $A_{\mathrm{E}} = W_{\mathrm{E}} \times L_{\mathrm{E}}$ is the effective emitter area; J_{S0} is the reverse saturation current density, η ($\geq$1) is the ideality factor, and V_{T0} is the thermal voltage, all at temperature T_0 = 300 K; ϕ [V/K] ($>$0) is the temperature coefficient of

V_{BEj} (in absolute value) and ΔT_{j} is defined as T_{j} - T_0, T_{j} being the (average) temperature over the base–emitter junction. This implies that Equation (5.9) accounts for the temperature dependence of I_{C} ($\approx I_{\mathrm{E}}$) making use of a V_{BEj} shift, by keeping J_{S0}, η, and V_{T0} at their T_0 values (e.g., [Zha96]). The ϕ dependence on I_{C} ($\approx I_{\mathrm{E}}$) can be described with the following logarithmic law [Nen04, dAl10, dAl14, dAl16, dAl17]:

$$\phi\left(I_{\mathrm{C}}\right) = \phi_0 - \eta\frac{k}{q}\ln\frac{I_{\mathrm{C}}}{A_{\mathrm{E}}J_{\mathrm{S0}}} \approx \phi_0 - \eta\frac{k}{q}\ln\frac{I_{\mathrm{E}}}{A_{\mathrm{E}}J_{\mathrm{S0}}} \tag{5.11}$$

Parameters J_{S0} and η in Equation (5.11) can be optimized by invoking the following procedure. First, the $I_{\mathrm{C}} - V_{\mathrm{BE}}$ characteristic of the DUT is measured at various thermochuck temperatures T_{B} under CE conditions by keeping V_{CE} small and sweeping V_{BE} up to values sufficiently low to reasonably neglect SH, HI, II, and resistive effects; as a consequence, the $I_{\mathrm{C}} - V_{\mathrm{BE}}$ curves can be modeled by:

$$I_{\mathrm{C}} = A_{\mathrm{E}}J_{S0}\exp\left[\frac{V_{\mathrm{BE}} + \phi\left(I_{\mathrm{E}}\right)\cdot\left(T_{\mathrm{B}} - T_0\right)}{\eta V_{\mathrm{T0}}}\right] \tag{5.12}$$

which stems from Equation (5.9) by considering $T_{\mathrm{j}} = T_{\mathrm{B}}$ and $V_{\mathrm{BEj}} = V_{\mathrm{BE}}$. Parameters J_{S0} and η are then tailored to match the experimental curve at $T_{\mathrm{B}} = T_0$ with

$$I_{\mathrm{C}} = A_{\mathrm{E}}J_{S0}\exp\left(\frac{V_{\mathrm{BE}}}{\eta V_{\mathrm{T0}}}\right) \tag{5.13}$$

and ϕ_0 is safely (SH is negligible) calibrated so as to ensure good agreement between all the $I_{\mathrm{C}} - V_{\mathrm{BE}}$ characteristics (at different T_{B}s) and the model given by Equation (5.12) with (5.11). Once ϕ_0 is known, Equation (5.11) can be used also at medium current levels, where the extraction of ϕ_0 would be inaccurate due to SH. Further details concerning the derivation of Equation (5.11), as well as the physical meaning of parameter ϕ_0, can be found in [dAl14]. Combining Equations (5.9) and (5.10), it can be obtained that:

$$V_{\mathrm{BE}} = R_{\mathrm{B}}I_{\mathrm{B}} + R_{\mathrm{E}}I_{\mathrm{E}} - \phi\left(I_{\mathrm{C}}\right)\Delta T_{\mathrm{j}} + \eta V_{\mathrm{T0}}\ln\frac{I_{\mathrm{C}}}{A_{\mathrm{E}}J_{\mathrm{S0}}} \tag{5.14}$$

By exploiting the thermal equivalent of Ohm's law, ΔT_{j} is expressed as:

$$\Delta T_{\mathrm{j}} = T_{\mathrm{j}} - T_0 = R_{\mathrm{TH}}P_{\mathrm{D}} + T_{\mathrm{B}} - T_0 \tag{5.15}$$

where P_{D} is the dissipated power. If $T_{\mathrm{B}} = T_0$, Equation (5.15) can be recast as:

$$\Delta T_{\mathrm{j}} = R_{\mathrm{TH}}P_{\mathrm{D}} = R_{\mathrm{TH}}\cdot\left(V_{\mathrm{BE}}I_{\mathrm{E}} + V_{\mathrm{CB}}I_{\mathrm{C}}\right) \approx R_{TH}\cdot\left(V_{\mathrm{BE}} + V_{\mathrm{CB}}\right)I_{\mathrm{E}} \tag{5.16}$$

wherein use has been made of the P_{D} expression in terms of applied or measurable voltages and currents under CB conditions. By substituting Equation (5.16) into (5.14),

$$V_{\mathrm{BE}} \approx \frac{R_{\mathrm{E}} I_{\mathrm{E}} - \phi\left(I_{\mathrm{E}}\right) R_{TH} V_{\mathrm{CB}} I_{\mathrm{E}} + \eta V_{T0} \ln \frac{I_{\mathrm{E}}}{A_{\mathrm{E}} J_{S0}}}{1 + \phi\left(I_{\mathrm{E}}\right) R_{TH} I_{\mathrm{E}}} \tag{5.17}$$

If a CB measurement is performed at $T_{\mathrm{B}} = T_0$ under a V_{CB} range limited to low values so as to avoid II effects, at a constant I_{E} sufficiently low to prevent HI and non-linear thermal effects, yet high enough to lead to perceptible SH, the (negative) slope γ of the $V_{\mathrm{BE}} - V_{\mathrm{CB}}$ characteristic is given by:

$$\gamma = \frac{dV_{\mathrm{BE}}}{dV_{\mathrm{CB}}} = -\frac{\phi\left(I_{\mathrm{E}}\right) R_{\mathrm{TH}} I_{\mathrm{E}}}{1 + \phi\left(I_{\mathrm{E}}\right) R_{\mathrm{TH}} I_{\mathrm{E}}} \tag{5.18}$$

whence the thermal resistance (R_{TH}) can be evaluated as [dAl10, dAl14, dAl16, dAl17, Kam17a]:

$$R_{\mathrm{TH}} = \frac{|\gamma|}{\left(1 - |\gamma|\right) \phi\left(I_{\mathrm{E}}\right) I_{\mathrm{E}}} \approx \frac{|\gamma|}{\phi\left(I_{\mathrm{E}}\right) I_{\mathrm{E}}} \tag{5.19}$$

In [dAl14], this improved approach was applied to about 100 single-emitter SiGe:C NPN BEC HBTs manufactured by IFX. The transistors are divided into three sets corresponding to different technology stages (and scaling strategies), which are hereinafter denoted as #1, #2, and #3. In particular, (i) set #2 is slightly scaled (both laterally and vertically) compared with #1; the collector current of HBTs belonging to #2 at peak f_{T} is about 30% higher than that of the #1 counterparts with approximately the same emitter area; (ii) set #3 devices underwent an aggressive lateral scaling with respect to #2 ones, while being vertically similar to them. The key figures of the sets are reported in Table 5.3. The thicknesses of the shallow and deep trenches are equal to 0.3 μm and 4.5 μm for all HBTs, respectively. For each set, transistors with several combinations of emitter width/length were available.

Table 5.3 Key figures of the analyzed IFX technology states

	#1	#2	#3
BV_{CBO} [V]	6.5–6.8	5.2–5.9	5.1–5.5
Peak f_{T} @ V_{CB} = 0 V [GHz]	190	225	235
J_{C} @ peak f_{T}, V_{CB} = 0 V [mA/μm^2]	6.5–7.0	9.0–9.5	9.5–10
Peak f_{T} @ V_{CB} = 0.5 V [GHz]	215	230	240
Peak f_{MAX} @ V_{CB} = 0 V [GHz]	250	310	330
Peak f_{MAX} @ V_{CB} = 0.5 V [GHz]	280	350	380

Figure 5.25 illustrates the experimentally extracted R_{TH}s as a function of L_E at assigned widths W_E for the three sets. It is shown that R_{TH} (i) significantly increases by reducing L_E and (ii) is well above 10^3 K/W and can grow beyond 10^4 K/W for small emitter areas. In particular, the smallest DUTs of sets #1 ($A_E = 0.2\times0.57\ \mu m^2$), #2 ($A_E = 0.14\times0.39\ \mu m^2$), and #3 ($A_E = 0.11\times0.63\ \mu m^2$) suffer from R_{TH} = 14,300, 21,000, and 22,000 K/W, respectively.

Numerical evidence of the accuracy of this technique was provided in [Kam17a], where it was applied to the simulation of an IFX SiGe:C DUT belonging to set #3 through an advanced tool solving the Boltzmann transport equations of electrons, holes, and longitudinal optical phonons, as well as the Energy Balance Equations for the other phonon modes (see Chapter 2).

5.4.2 Thermal Simulation

A viable strategy to assess the impact of technology on the thermal behavior of SiGe HBTs involves the adoption of 3-D finite-element method (FEM) thermal simulations, which are suited to handle structures with arbitrarily complex geometries [Rei01, Wal02].

An interesting contribution has been given in [Sah13], where non-linear steady-state, large signal, and sinusoidal thermal analyses of an STM SiGe:C HBT (with drawn emitter area equal to 0.27 $\mu m \times 10\ \mu m$) were carried out with Sentaurus; the thermal resistance was found to be in fairly good agreement with the one measured according to the procedure in [Pfo03], although no thermal conductivity degradation mechanisms (e.g., due to high doping) were accounted for. The Back-End-Of-Line (BEOL) structure was found to play a marginal role due to the absence of the metal-via stack above the emitter. This analysis has been recently extended to cover the influence of BEOL on the thermal behavior of multi-finger devices, with emphasis on the coupling among fingers [Dwi16].

In [dAl10], the software package Comsol [Com] was adopted to analyze SH in several STM SiGe:C HBTs. In spite of their geometrical complexity, the devices were reproduced with a very high accuracy up to the emitter, base, and collector contacts, the top surfaces of which were considered adiabatic, that is, the BEOL architecture was not included. Unfortunately, although the upward heat flow was unrealistically suppressed, the numerical R_{TH}s were found to *underestimate* by about 20–25% the experimental values determined through the technique described in the section "Experimental R_{TH} Extraction," independently of technology stage and emitter size. An improved

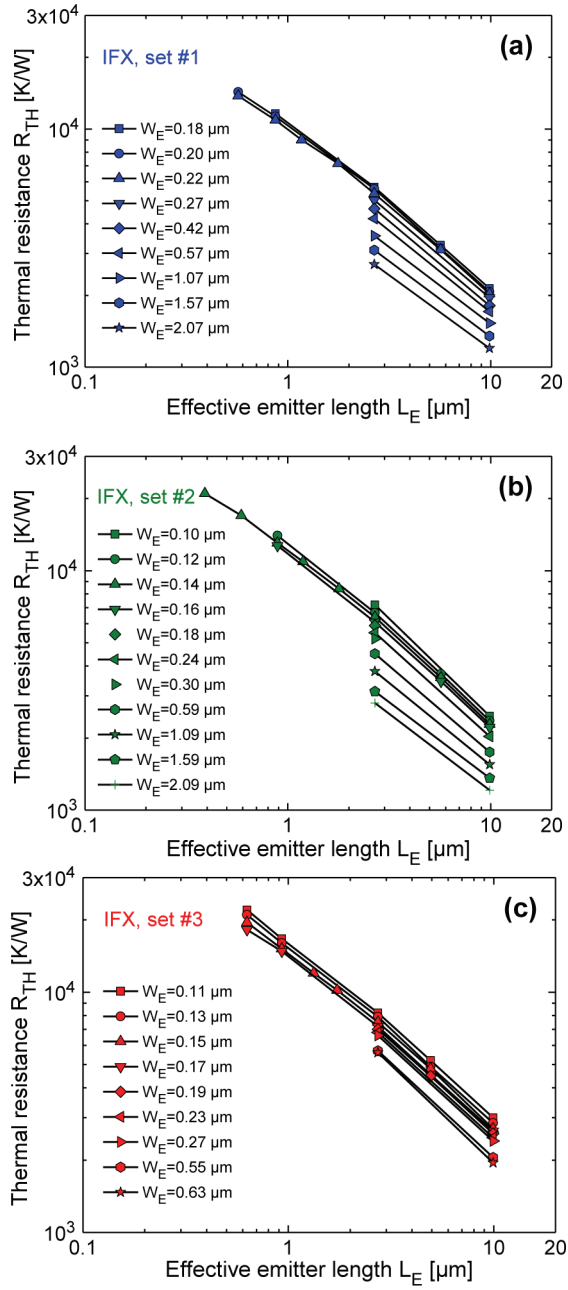

Figure 5.25 Thermal resistance (R_{TH}) as a function of emitter length (L_{E}) for various emitter widths (W_{E}), as experimentally determined for sets (a) #1, (b) #2, and (c) #3.

variant of the approach in [dAl10] was applied to IFX transistors in [dAl16]. The advances with respect to [dAl10] are reported below:

- The whole BEOL structure, comprising five metal (copper) layers and related interconnections (copper vias between metal layers, tungsten contacts between silicon and the lowest metal layer), was taken into account, as well as the external pads, as witnessed by Figure 5.26 reporting the Comsol grid. This allows quantifying the cooling influence due to the upward heat flow (often disregarded in the literature), which is expected to be relevant since – differently from the STM transistor analyzed in [Sah13] – a metal-via stack is located over the emitter in the IFX DUTs.
- In bipolar transistors, the power dissipation occurs at the base–collector SCR. In conventional approaches for thermal simulations, for a rectangular emitter window, such a region is modeled as either a rectangular or a parallelepiped heat source (e.g., [dAl10, Sah13]), both with uniform power density. In [dAl16], the dissipation region is more accurately modeled by resorting to 2-D electrical simulations of the DUTs preliminarily performed with Sentaurus in order to determine a realistic power density distribution; for this aim, the hydrodynamic model with transport parameters optimized for SiGe:C HBTs [Sas10] was used. By referring to the schematic cross section of the DUTs represented in Figure 5.27, the heat sources exploited in the Comsol structures were built with the power density pattern obtained by reproducing the distribution computed by Sentaurus in the (x, z) plane and assuming a

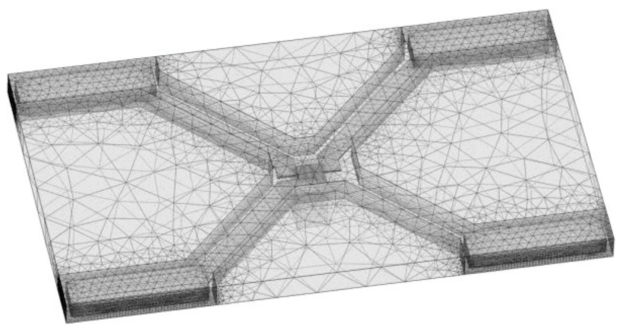

Figure 5.26 Detail of the 3-D Comsol mesh for the IFX transistor with $A_{\mathrm{E}} = 0.13 \times 2.73\ \mu\mathrm{m}^2$, composed of 1.35 million tetrahedra of grossly different dimensions, corresponding to 1.8 million degrees of freedom.

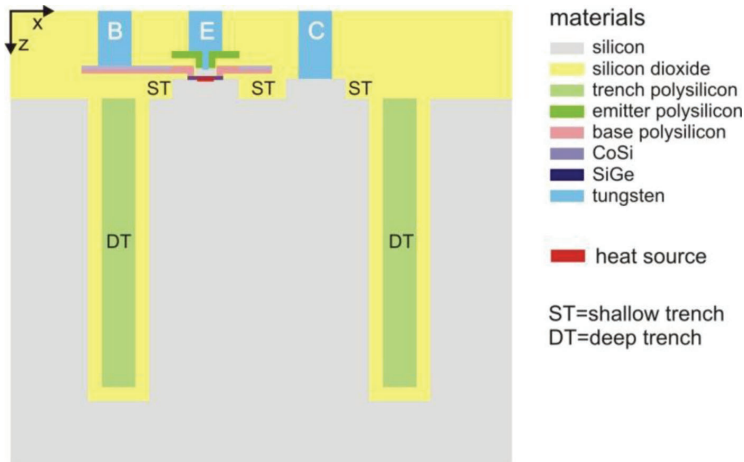

Figure 5.27 Schematic representation (limited to the innermost tungsten contacts) of the typical cross section of the IFX DUTs.

uniform density along the device length (i.e., along the *y*-axis orthogonal to the cross section).

- Thermal simulations are usually performed by setting the thermal conductivities k [W/mK] of the materials to values measured from "bulk" samples (listed in Table 5.4). However, in practical cases, many effects concur to reduce k, which can be even position-dependent within the same material. In the SiGe alloy, k is a function of the z-dependent Ge mole fraction x_{Ge} according to the law [Pal04]

$$k_{\mathrm{SiGe}} = \left[\frac{1 - x_{\mathrm{Ge}}}{k_{\mathrm{Si}}} + \frac{x_{\mathrm{Ge}}}{k_{\mathrm{Ge}}} + \frac{(1 - x_{\mathrm{Ge}})\, x_{\mathrm{Ge}}}{c_{\mathrm{k}}} \right]^{-1} \tag{5.20}$$

Table 5.4 Bulk thermal conductivities

Material	Bulk Thermal Conductivity [W/mK]
Silicon	148
Germanium	60
Silicon dioxide	1.4
Tungsten	177
Copper	390
Emitter polysilicon	40
Base polysilicon	30
Trench polysilicon	20
Cobalt silicide	9.6

where k_{Si} and k_{Ge} are the thermal conductivities of pure Si and Ge, respectively, and c_{k} is a bowing factor equal to 2.8 W/mK. Due to the k lowering imposed by Equation (5.20), the SiGe layer behaves as a barrier for the heat flow from the heat source to the emitter [Pet15]. The thermal conductivity is also adversely impacted by doping due to the enhanced phonon-impurity scattering, as experimentally observed in [Sla64, McC05, Lee12]; a compact formulation to account for this effect is [Lee12]:

$$k_{\mathrm{Si,doped}}\left(k_{\mathrm{SiGe,doped}}\right) = \frac{k_{\mathrm{Si}}\left(k_{\mathrm{SiGe}}\right)}{1 + A \cdot \left(\frac{N}{N_{\mathrm{norm}}}\right)^{\alpha}} \tag{5.21}$$

where N [cm^{-3}] is the position-dependent total doping concentration (acceptors and donors), N_{norm} = 10^{20} cm^{-3}, while the values of the parameters are A = 0.74186, α = 0.7411 for boron [Lee12], and A = 1.698, α = 0.8251 for arsenic, as obtained with a calibration procedure relying on experimental results provided in [McC05]. Lastly, the heat propagation through laterally thin layers can be significantly jeopardized by the phonon scattering with the layer boundaries [Liu05]. In SiGe HBTs, where the heat flow is mostly vertical, scattering mechanisms – expected to be exacerbated in narrow (low-W_{E}) transistors – can take place along device portions like (from the top) emitter tungsten contact, Si emitter, SiGe base, and Si volume surrounded by ST. This deleterious effect can be included by using, e.g., the simple analytical method proposed in [Tor00], which leads to a reduced anisotropic thermal conductivity with x-dependent components given by:

$$\begin{aligned}\frac{k_{\mathrm{y,z}}(x')}{k_{\mathrm{Si,doped}}\left(k_{\mathrm{SiGe,doped}},k_{\mathrm{contact}}\right)} = \; & 1 - \tfrac{1}{2}\exp\left[-\left(\frac{x'}{x_{\mathrm{charyz}}}\right)^{0.75}\right] \\ & -\tfrac{1}{2}\exp\left[-\left(\frac{1-x'}{x_{\mathrm{charyz}}}\right)^{0.75}\right]\end{aligned} \tag{5.22}$$

$$\begin{aligned}\frac{k_{\mathrm{x}}(x')}{k_{\mathrm{Si,doped}}\left(k_{\mathrm{SiGe,doped}},k_{\mathrm{contact}}\right)} = \; & 1 - \tfrac{1}{2}\exp\left[-\left(\frac{x'}{x_{\mathrm{charx}}}\right)^{0.95}\right] \\ & -\tfrac{1}{2}\exp\left[-\left(\frac{1-x'}{x_{\mathrm{charx}}}\right)^{0.95}\right]\end{aligned} \tag{5.23}$$

where x' = x/W, W being the layer width (along y), x_{charyz} = 0.32 $\cdot$ Λ/W and x_{charx} = 0.72 $\cdot$ Λ/W, Λ being the mean free path for phonons (equal to 300 nm in Si and SiGe layers, and to 40 nm in the tungsten emitter contact).

It must be remarked that only Equation (5.20) was accounted for in [dAl10].

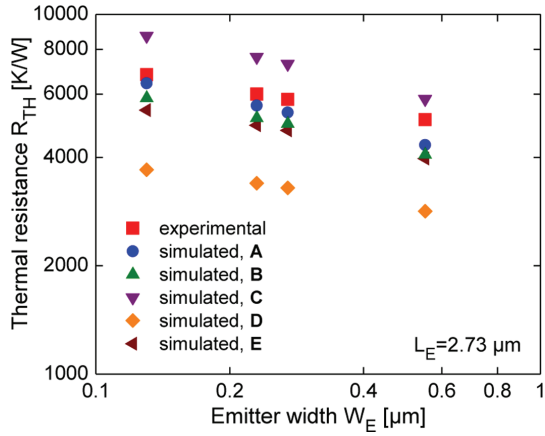

Figure 5.28 Thermal resistances as a function of emitter width for IFX devices sharing L_E = 2.73 μm: experimental (squares) values are compared with those calculated through the simulation approaches **A** (circles), **B** (triangles), **C** (flipped triangles), **D** (rhombi), and **E** (left-oriented triangles).

As discussed in [dAl16], Comsol steady-state simulations were performed by applying an adiabatic boundary condition at the top and lateral faces of the structure, and an isothermal condition on the backside ($T_B = T_0$). The thermal resistance was determined by evaluating the average of the temperature field over the base–emitter junction, which mostly influences the behavior and performance of the device [Zha96], subtracting T_0 and normalizing to the dissipated power (P_D). Results corresponding to DUTs with different W_Es and sharing L_E = 2.73 μm are reported in Figure 5.28, which shows:

- the R_{TH}s determined through the improved experimental technique outlined in the section "Experimental R_{TH} Extraction";
- the R_{TH}s simulated with Comsol by considering the full advanced approach described above (denoted as approach **A**), i.e., by including the BEOL architecture and accounting for the non-uniform power density pattern and the conductivity degradation mechanisms;
- the R_{TH}s calculated with Comsol by modeling the power dissipating region through a standard parallelepiped-shaped source with uniform power density, while considering all other effects and the BEOL structure (approach **B**);
- the R_{TH}s computed with Comsol by accounting for a heat source with non-uniform power density and replacing the metal in the BEOL

architecture with SiO_2 so as to virtually exclude it, while including the first-level tungsten contacts only (approach **C**);
- the R_{TH}s evaluated with Comsol by restoring the BEOL, and considering uncorrected "bulk" values for the thermal conductivities and a standard parallelepiped-based heat source (approach **D**);
- the R_{TH}s computed with Comsol by disregarding the above effects and excluding the BEOL so as to emulate a traditional simulation technique (approach **E**).

By using approach **A**, the R_{TH} of the device with W_E = 0.13 μm was calculated to be 6,437 K/W, which is in fairly good agreement (–5.3%) with the experimental value (6,800 K/W); conversely, a relatively high underestimation (–15%) was obtained for the widest (W_E = 0.55 μm) device, the numerical and measured R_{TH}s being 4,333 K/W and 5,100 K/W, respectively. A post-processing analysis revealed a markedly non-uniform temperature distribution along x over the base–emitter junction compared to low-W_E transistors, which can be ascribed to the concurrent action of the low k_{SiGe} and the narrow tungsten emitter contact (the width of which does not scale with W_E). As a consequence, the evaluation of R_{TH} with a standard geometrical ΔT_j average over the whole junction is likely to be incorrect, and the accuracy should be improved by developing more complex averaging approaches that would lead to a higher FEM R_{TH}. If approach **B** (with the traditional heat source representation) is adopted, the numerical R_{TH} lowers (compared to **A**) from –9% for the HBT with W_E = 0.13 μm to –5.9% for the one with W_E = 0.55 μm, where the base–emitter temperature is non-uniform. Hence, it can be stated that the heat source representation plays a significant role. By making use of the BEOL-free approach **C** (upward heat flow almost annihilated), the FEM R_{TH} of the transistor with W_E = 0.13 μm grows to 8,712 K/W, which corresponds to +28% with respect to the experimental value; this means that, although the low-conductivity SiGe base and Si emitter concur to limit the upward heat flow, the BEOL effectively extracts heat from the emitter. This mechanism is also amplified by the doping-affected conductivity of sub-collector, which counteracts the downward heat propagation. Similar considerations hold for the other narrow HBTs, whereas for the device with W_E = 0.55 μm the lower overestimation (+14%) can be again attributed to the too simple geometrical averaging procedure for the junction temperature field. By exploiting approach **D**, the DUTs enjoy an exacerbated cooling effect dictated by the BEOL architecture and the adoption of the "bulk" thermal conductivity of Si, which favor both the

downward and upward heat flow. Consequently, the FEM R_{TH}s are far lower (about –45%) than the experimental counterparts. As expected, employing the traditional approach **E** leads to an underestimation of about –20% regardless of W_{E}, since the deactivation of the k reduction mechanisms (which would imply a heating effect) prevails over the BEOL absence (which would instead cool down the device).

5.4.3 Scaling Considerations

Thermal effects in SiGe HBTs still need to be included in the circuit design process via suitable compact models, which require a geometry-scalable lumped description of the thermal resistance, i.e., an expression of R_{TH} as a function of W_{E} and L_{E} for a given technology stage.

The following simple law was proposed for HICUM/L2 [Sch13]:

$$R_{\mathrm{TH}} = \frac{R_{\mathrm{TH0}}}{1 + a_{\mathrm{W}} W_{\mathrm{E}} + a_{\mathrm{L}} L_{\mathrm{E}}} \tag{5.24}$$

where R_{TH0} [K/W], a_W [$\mu\mathrm{m}^{-1}$], a_{L} [$\mu\mathrm{m}^{-1}$] are fitting parameters. Another formulation, conceived for Mextram504, relies on the preliminary knowledge (from experiments) of the thermal resistance (R_{THref}) of a reference transistor, and three dimensionless fitting parameters (b_A, b_{W}, b_{L}) to be calibrated [Wu06a, Wu06b]:

$$R_{\mathrm{TH}} = \frac{R_{\mathrm{THref}}}{1 + b_{\mathrm{A}} \left(\frac{W_{\mathrm{E}} L_{\mathrm{E}}}{W_{\mathrm{Eref}} L_{\mathrm{Eref}}} - 1 \right) + b_{\mathrm{W}} \left(\frac{W_{\mathrm{E}}}{W_{\mathrm{Eref}}} - 1 \right) + b_{\mathrm{L}} \left(\frac{L_{\mathrm{E}}}{L_{\mathrm{Eref}}} - 1 \right)} \tag{5.25}$$

Lastly, a more sophisticated model was developed by resorting to the following procedure. The exact closed-form solution to the heat transfer equation for a rectangle-shaped indefinitely-thin heat source (THS) with area $W_{\mathrm{E}} \times L_{\mathrm{E}}$ located on the adiabatic top surface of a semi-infinite homogeneous "bulk" domain (with thermal conductivity k) is given by [Rin00]

$$R_{\mathrm{TH}} = \frac{1}{2\pi k} \left[\frac{1}{L_{\mathrm{E}}} \ln \left(\frac{L_{\mathrm{E}} + \sqrt{W_{\mathrm{E}}^2 + L_{\mathrm{E}}^2}}{-L_{\mathrm{E}} + \sqrt{W_{\mathrm{E}}^2 + L_{\mathrm{E}}^2}} \right) + \frac{1}{W_{\mathrm{E}}} \ln \left(\frac{W_{\mathrm{E}} + \sqrt{W_{\mathrm{E}}^2 + L_{\mathrm{E}}^2}}{-W_{\mathrm{E}} + \sqrt{W_{\mathrm{E}}^2 + L_{\mathrm{E}}^2}} \right) \right] \tag{5.26}$$

It is worth noting that the width and length of the THS were assumed to coincide with the emitter ones, which is a reasonable assumption. Unfortunately, Equation (5.26) with k = 148 W/mK (thermal conductivity of Si, as can be seen in Table 5.4) revealed to be unsuited for SiGe HBTs: the R_{TH} values were found to be about 65–75% lower than the experimental counterparts (addressed later) although the cooling effect due to the upward heat flowing to the BEOL structure is not modeled. This means that the heating effect caused by the shallow/deep trenches filled with low thermal conductivity materials – not included in Equation (5.26) as well – plays a role more important than BEOL. Equation (5.26) can be recast in the form:

$$R_{\mathrm{TH}} = \frac{1}{2\pi k}\left[\frac{1}{L_{\mathrm{E}}}\ln\left(\frac{1+\sqrt{\left(\frac{W_{\mathrm{E}}}{L_{\mathrm{E}}}\right)^2+1}}{-1+\sqrt{\left(\frac{W_{\mathrm{E}}}{L_{\mathrm{E}}}\right)^2+1}}\right)+\frac{1}{W_{\mathrm{E}}}\ln\left(\frac{\frac{W_{\mathrm{E}}}{L_{\mathrm{E}}}+\sqrt{\left(\frac{W_{\mathrm{E}}}{L_{\mathrm{E}}}\right)^2+1}}{-\frac{W_{\mathrm{E}}}{L_{\mathrm{E}}}+\sqrt{\left(\frac{W_{\mathrm{E}}}{L_{\mathrm{E}}}\right)^2+1}}\right)\right] \tag{5.27}$$

If $W_{\mathrm{E}}/L_{\mathrm{E}} \ll 1$, the square root can be approximated with a first-order Taylor series expansion

$$\sqrt{\left(\frac{W_{\mathrm{E}}}{L_{\mathrm{E}}}\right)^2+1} \approx 1+\frac{1}{2}\left(\frac{W_{\mathrm{E}}}{L_{\mathrm{E}}}\right)^2 \tag{5.28}$$

By substituting Equation (5.28) into (5.27) and neglecting the second-order terms, it is found that:

$$R_{\mathrm{TH}} \approx \frac{1}{2\pi k}\left\{\frac{2}{L_{\mathrm{E}}}\ln\left(2\frac{L_{\mathrm{E}}}{W_{\mathrm{E}}}\right)+\frac{1}{W_{\mathrm{E}}}\left[\ln\left(1+\frac{W_{\mathrm{E}}}{L_{\mathrm{E}}}\right)-\ln\left(1-\frac{W_{\mathrm{E}}}{L_{\mathrm{E}}}\right)\right]\right\} \tag{5.29}$$

Finally, by expressing also the logarithms with a first-order Taylor series expansion, after some algebra,

$$R_{\mathrm{TH}} \approx \frac{1}{\pi k L_{\mathrm{E}}}\left[\ln\left(2\frac{L_{\mathrm{E}}}{W_{\mathrm{E}}}\right)+1\right] \tag{5.30}$$

Equation (5.30) represents a good approximation of the *exact* (5.26) for heat sources with medium/high aspect ratio $W_{\mathrm{E}}/L_{\mathrm{E}}$, while slightly losing accuracy

when $W_E \rightarrow L_E$. It was empirically demonstrated that Equation (5.30) can be extended to a wider range of W_E values by introducing a correction term equal to 0.12 in the logarithm argument, which leads to:

$$R_{TH} = \frac{1}{\pi k L_E}\left[\ln\left(0.12 + 2\frac{L_E}{W_E}\right) + 1\right] \tag{5.31}$$

In order to potentially predict the L_E and W_E dependence of the R_{TH} for SiGe HBTs of a specific technology stage, Equation (5.31) was further generalized to [dAl14]:

$$R_{TH} = \frac{1}{\pi k L_E}\left[\ln\left(c + c_R\frac{L_E}{W_E}\right) + 1 + \frac{c_W}{W_E}\right] \tag{5.32}$$

where c, c_R, c_W and the thermal conductivity (k) are fitting parameters. In particular, the term c_W/W_E was introduced to ensure a good fitting over a broad W_E span. It must be remarked that considering k as a fitting parameter has physically sense in SiGe HBTs, since the heat emerging from the dissipation region propagates through various materials with different thermal conductivities (e.g., Si, SiGe, poly, oxide, and tungsten). Models (5.24), (5.25), and (5.32) with optimized parameters (see Table 5.5) were compared to experimental data determined with the approach described in the section "Experimental R_{TH} Extraction" on set #2 devices for various W_Es and three emitter lengths in Figure 5.29.

Results can be summarized as follows: law (5.24) relying on three fitting parameters (the calibrated R_{TH0} is well above the range of the experimental R_{TH}s, and thus cannot be interpreted as a real thermal resistance) and (5.25) based on three fitting parameters plus a "reference" (measured) thermal resistance are suited to offer a fairly good matching with experimental data within a wide range of L_E and W_E values. Excellent agreement is provided by (5.32), which is an extended version of a formulation derived for homogeneous "bulk" domains, and makes use of four fitting parameters, one of which is thermal conductivity. Interestingly, it was found that the optimized k value

Table 5.5 Optimized parameters of the scalable R_{TH} models

Model	Parameters			
(5.24)	R_{TH0} = 34,893 K/W	a_W = 4.46 μm^{-1}		a_L = 1.44 μm^{-1}
(5.25)	R_{THref} = 3,570 K/W ($W_E \times L_E$ = 0.14 × 5.69 μm^2)	b_A = 0.034	b_W = 0.045	b_L = 0.792
(5.32)	c = 0.97	c_R = 1.265	c_W = 0.0166	k = 80 W/mK

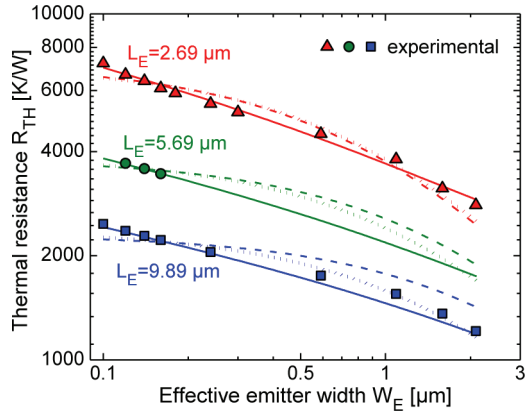

Figure 5.29 Comparison between scalable models (5.24) (dashed lines), (5.25) (dotted), (5.32) (solid) with calibrated parameters, and experimental R_{TH}s (symbols) for set #2 transistors.

(80 W/mK) is lower than the Si counterpart, which is physically reasonable since the lateral heat propagation is mostly influenced by shallow/deep trenches filled with the low-conductivity materials like poly and oxide.

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