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(Sub)mm-wave Calibration

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4.1 Introduction

High-frequency characterization of active and passive devices is carried out by extracting the scattering parameters of the component (often in a two-port configuration) employing a vector network analyzer (VNA). This class of instruments allows to characterize the response of the device under test (DUT) over a broad frequency range (exceeding 1 THz [Dio17]) at a user-defined reference plane. In order to define such reference planes and remove all the imperfections of the measurement setup (i.e., cable and receiver conversion losses, amplitude and phase tracking errors, and other statistical errors), a calibration procedure [Ryt01] needs to be carried out prior to the measurement. The calibration procedure employs the knowledge of the devices used (i.e., standards) to solve the unknowns representing the measurement setup response (often referred to as error terms). The derived error terms allow then to remove the imperfections of the setup, during the measurement procedure. The accuracy of the calibration is then directly dependent on the accuracy with which the standards are known [Stu09]. In the literature, different calibration techniques have been presented, often trading off (more) knowledge on the response of the standard device for (lower) space occupancy (i.e., when considering SOLR/LRM [Fer92; Dav90] calibrations versus TRL type ones [Eng79]). Traditionally, calibration techniques requiring little standards knowledge (e.g., TRL, LRL) have been considered the most accurate, with TRL reaching metrology institute precision, by only requiring the information of the characteristic impedance of the line [Eng79]. In this chapter the focus will be placed only on TRL calibration techniques due to their best compatibility with millimeter- and sub-millimeter-wave

characterization. For a more extensive discussion on the various possible calibration techniques the reader is referred to [Tep13]. Calibration techniques for on-wafer measurements typically consist of a probe-level calibration (first-tier) performed on a low-loss substrate (i.e., alumina or fused silica) [Eng79; Eul88; Dav90; Mar91a]. This probe-level calibration is then transferred to the environment where the DUT is embedded in and often, to increase the measurement accuracy, this calibration is augmented with a second-tier on-wafer calibration/de-embedding step. This allows moving the reference plane as close as possible to the DUT, by removing the parasitics associated with the contact pads, the device-access lines, and the vias [Tie05]. In this chapter we will first review the challenges and potential solutions associated with first-tier calibrations performed on low-loss substrates, then the approach to design calibration kits integrated in the back-end-of-line of silicon based technology will be presented, and finally a direct de-embedding/calibration strategy, capable of setting the reference plane at the lower metal layer of a technology stack, will be described.

4.2 Multi-mode Propagation and Calibration Transfer at mm-wave

The different propagating modes supported by a coplanar wave guide (CPW) are qualitatively sketched in Figure 4.1. The CPW mode, characterized by opposite direction of the fields across the slots, represents the intended propagation mode and is often referred to as *CPW differential mode.* The CPW mode characterized by in-phase direction of the fields across the slots (W_{GAP}) represents an unwanted radiating mode and is often referred to as *CPW common mode.* The TM_{n} and TE_{m} modes are surface waves propagating along the grounded dielectric slab. Their cut-off frequencies

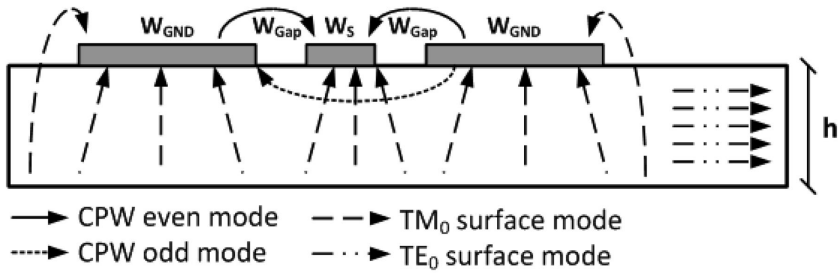


Figure 4.1 Cross section of a coplanar wave guide (CPW) with finite ground planes, and sketches of the E field distributions of the first propagating modes supported.

($n > 0$ and $m \geq 1$) are functions of the height and dielectric constant of the substrate [Poz04]. The overall effect of the unwanted modes described above is an increase of the transmission line losses (i.e., $|S_{21}|$) and the generation of ripples on the transmission parameter (i.e., S_{21}) of the CPW. The ripples are the results of interference (constructive or destructive depending on the frequency) between the unwanted modes, reflected by discontinuities (i.e., dielectric constant changes), and the intended CPW mode. The lines conventionally employed for probe-level TRL calibrations, are:

- *The thru standard:* A CPW line with a physical length in the order of 200–250 μm,
- *The line standard:* A CPW line providing an insertion phase of 90° at the center of the calibration band.

The analysis presented in this section is based on numerical 3D EM simulations, i.e., using Keysight EM Pro.

4.2.1 Parallel Plate Waveguide Mode

During the calibration procedure the substrate is placed on a metallic wafer chuck, creating effectively a grounded coplanar waveguide (GCPW) structure, as shown in Figure 4.2(a–c). This structure supports, in addition to the modes shown in Figure 4.1, also a parallel plate waveguide (PPW) mode.

This occurs since the top (CPW line) and bottom (chuck) metal are not directly contacted, thus a different potential can exist and propagate. The PPW mode can be visualized by plotting the E field intensity below the metal surface, as shown in Figure 4.2(c–d). In the figure the intensity of the E field is acquired on the xy plane placed below the metal plane (i.e., 5 μm). Note, both plots use the same range for the field intensity (blue = minimum, red = maximum) to allow for a direct visual comparison. Conventionally to reduce the PPW mode propagation, an interposer substrate of ferromagnetic material (i.e., providing high losses for the EM waves) is used between the calibration substrate and the metal chuck. Figure 4.2(d) shows a partial reduction of the PPW mode when simulating with the absorber structure. Alternatively, dielectric chucks with a permittivity similar to the one of the calibration substrate can be used to remove the occurrence of the PPW mode.

4.2.2 Surface Wave Modes: TM_0 and TE_1

The overall loss behavior of the CPW structure, including the surface waves when fed by a wafer probe, can be analyzed by using the 3D simulation environment shown in the inset of Figure 4.3(a). A point voltage source with

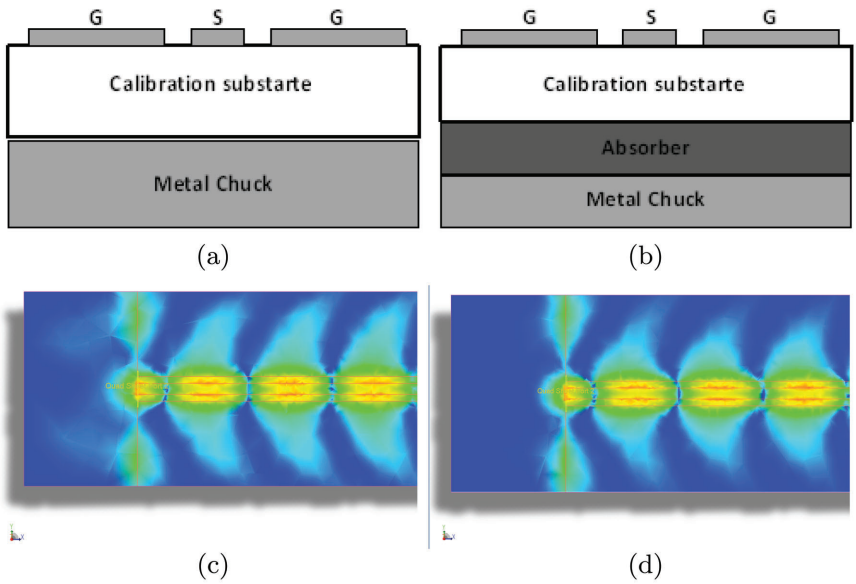


Figure 4.2 Cross section of CPW placed (a) on metal chuck, (b) on absorber. Electrical field intensity below the CPW metal plates (5 μm) for case (c) no absorber and (d) with absorbing boundary conditions in the 3D FEM simulation, both fields were computed at 180 GHz.

a source impedance of 50 Ohm is applied to the bridge to provide a transition similar to a wafer probe. In the 3D simulation environment, the boundary conditions were set to absorbing, thus providing perfect match condition to all the unwanted modes within the structure.

Figure 4.3(a) compares the insertion loss of the CPW structure realized in alumina when the substrate (sub) is enlarged and an air gap (GAP) is applied between the substrate boundary and the radiation boundary of the box, see Figure 4.3(b). Note that the multiple reflections of the unwanted modes within the structure generate an interference pattern (dependent on the distance to the discontinuity) along the trace, as can be seen by the shift of minima and maxima points when the sub-parameter is changed. The simulation does not include conductive or dielectric losses thus the decrease in the transmission parameter S_{21} in Figure 4.3(a) can only be attributed to energy dissipated in the other modes supported by the structure. When considering real structures on alumina substrate (i.e., exhibiting also dielectric losses), it is expected that the lines closer to the edge of the calibration substrate will exhibit a stronger ripple caused by interference with the surface wave mode. In Figure 4.3(b) structures with different distance to the substrate edge where

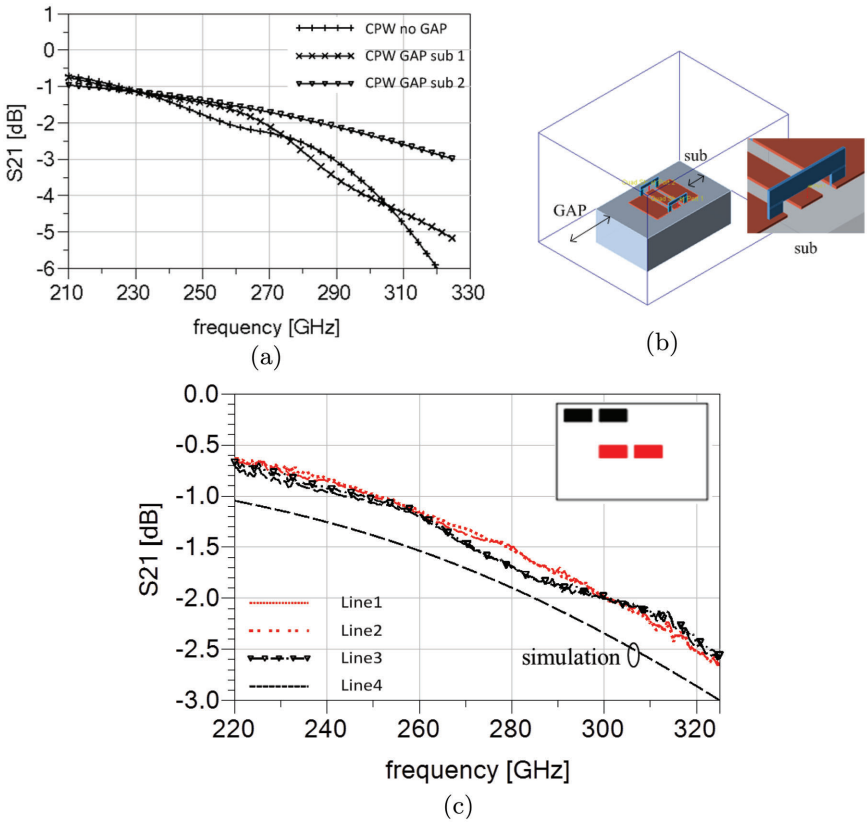


Figure 4.3 (a) Simulated S_{21} of CPW on alumina substrate for various cases: *CPW no GAP* sub $= 0\ \mu$m GAP $= 0\ \mu$m, *CPW GAP sub1* sub $= 320\ \mu$m GAP $= 500\ \mu$m, *CPW GAP sub2* sub $= 420\ \mu$m GAP $= 500\ \mu$m; (b) CPW structure used in the EM simulator with highlight on the lumped bridge configuration; (c) measurement of different (4) thru lines on alumina substrate in different locations of the calibration substrate. Locations (i.e., two middle and two center) identified in the inset on top right.

measured (i.e., center and edge) for the alumina substrate. As can be clearly seen by the figure, the structures at the edge of the substrate exhibit a clear interference pattern, as predicted by the simulation analysis.

4.2.3 Electrically Thin Substrates

Employing lower ϵ_r substrates shifts the occurrence of the TM_1 and TE_1 modes to higher frequencies, and reduces the amount of energy radiated by the CPW common mode, for a given frequency, due to the smaller gap

dimension for a given signal width. For these reasons, fused silica ϵ_r can be considered as a good candidate to integrate CPWs to perform TRL calibration in the (sub)mm-wave bands. The same simulation analysis performed for the alumina case in Figure 4.3(a) was carried out for the fused silica substrate, see Figure 4.4(a). As can be seen by the plot a considerably lower amount of energy is transferred to other modes. Moreover, the lower dielectric constant of the substrate provides lower discontinuities when terminated with air, showing close to no-variation when performing a simulation varying the dimension of the parameters sub and GAP, see Figure 4.4(a).

The measured results are then compared with the simulation showing very good agreement in WR3 band, as shown in Figure 4.4(b), confirming also the low loss achieved by the CPW realized on fused silica. Note, that the deviation that can be observed between measured and simulated data above 290 GHz can be explained with reduced sensitivity of the measurement equipment, closer to the edge of the specified band (i.e., WR3 220–325 GHz) and the onset of unwanted modes in the fused silica substrate.

4.2.4 Calibration Transfer

In the previous paragraph the usage of electrically thin substrates was introduced to overcome the limitations exhibited by commercially available calibration devices operating in the mm-wave bands. While using such substrates (i.e., fused silica) improves the calibration quality, an important point is that the measurement quality will also depend on the error introduced by transferring the calibration to the environment where the DUT is embedded.

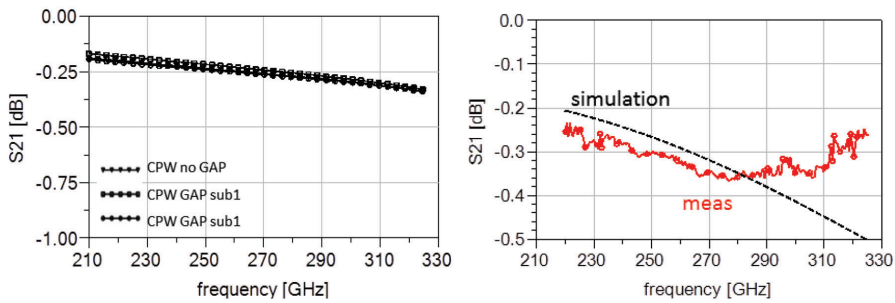


Figure 4.4 (a) Simulated S_{21} of CPW on fused silica substrate for various cases: *CPW no GAP* sub $=$ 0 μm GAP $=$ 0 μm, *CPW GAP sub1* sub $=$ 320 μm GAP $=$ 500 μm, *CPW GAP sub2* sub $=$ 420 μm GAP $=$ 500 μm; (b) measurement versus simulation of a thru line on fused silica substrate.

It is often the case that the DUT is embedded in a different host medium compared to the calibration, i.e., *Si, SiO_2, GaAs*, or other substrate materials. When the measurement is performed on the new host medium, a different probe to substrate interaction will occur, which would not be corrected for by the calibration. This will introduce a residual error that would be a function of the difference in permittivity between the two substrate materials (i.e., calibration and measurement). In a first-order approximation, the calibration transfer effect, associated with the change in the error box, can be seen as a capacitive coupling between the probe tip and the substrate, as schematized in Figure 4.5. This capacitance can be found using a numerical optimizer when the probe geometry is partially known, allowing to minimize the calibration transfer error in the measurement frequency band.

Figure 4.6 shows the results, in terms of worst case of the error bound [Wil92], when transferring the calibration from the primary calibration environment (i.e., alumina and fused silica) to a verification line embedded in the back-end-of-line of a SiGe high-speed process. The calibration quality is evaluated before any optimization is applied (full symbols and solid lines) and after the application of the correction (empty symbols, dotted lines). The maximum value for the error associated with the calibration of alumina decreased from 0.12 to 0.06, with an improvement noticeable over the entire bandwidth. However, no significant improvement is obtained for the fused

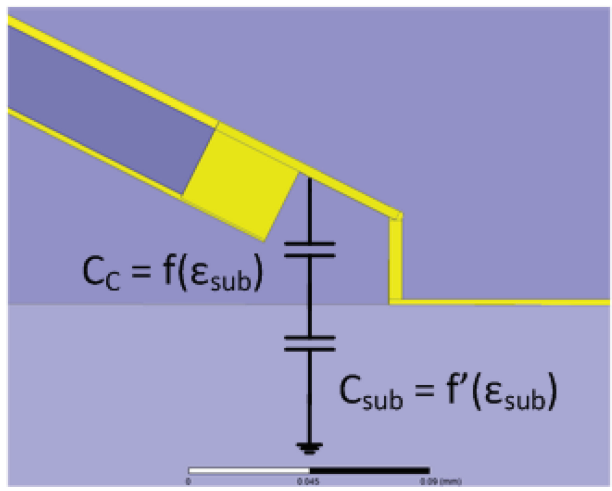


Figure 4.5 Schematic representation of the capacitive coupling between the probe tip and the substrate where the device under test (DUT) is embedded.

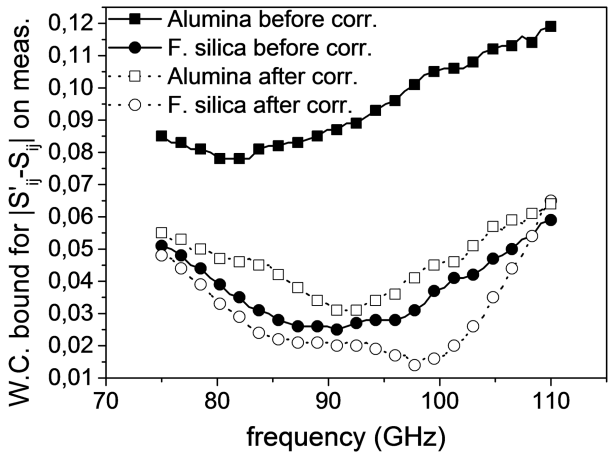


Figure 4.6 Worst case error bound for calibration transfer from fused silica and alumina to SiGe BEOL, before correction (full symbols, solid lines) and after correction (empty symbols, dotted lines), obtained with on-wafer measurements on a 600 μm CPW line manufactured on IHP SiGe 130 nm BiCMOS technology, in the frequency range from 75 to 110 GHz.

silica, where the error associated with the difference in substrate coupling due to calibration transfer is small, due to the similarity of permittivity between the fused silica and the silicon dioxide present in the back-end-of-line of the process.

4.3 Direct On-wafer Calibration

In order to avoid the error arising from the process of transferring the first-tier calibration to another environment, the calibration kit should be implemented in the same environment as that of the DUT. Classical probe-level and on-wafer calibration techniques are based on (partially) known devices and lumped models of the DUT fixture (i.e., SOLT/LRM and lumped de-embedding) or employ distributed concepts (TRL and multi-line TRL). Due to the objective difficulty, especially at higher frequencies, in manufacturing an accurate and predictable resistor in a commercial silicon technology, (multiline)-TRL calibration represents the standard employed technique for *in situ* calibration, as was shown in [Yau10; Yau12; Wil13a; Wil13b; Wil14]. The TRL technique does not require resistors to define the measurement normalization impedance, which is instead set by the characteristic impedance of the lines used during the calibration. Thus, the accurate

(frequency-dependent) determination of the calibration lines characteristic impedance becomes a key requirement to allow the correct re-normalization of TRL-calibrated S-parameter measurements.

4.3.1 Characteristic Impedance Extraction of Transmission Lines

To accurately employ TRL techniques in a complex environment such as the BEOL of Silicon-based technologies, a robust approach is required to extract the characteristic impedance of the transmission line. Traditional extraction procedures are based on measurements [Eis92; Mar91a; Wil91a; Wil91b; Mar91b; Wil98], but are only accurate when specific assumptions are verified, such as, low loss substrate, constant capacitance per unit length [Mar91b], and uniform [Eis92] non-inductive pad-to-line transitions [Wil98; Wil01]. For a more extensive analysis of the shortcomings of these methods for (sub)-mm-wave calibration in the BEOL of silicon technologies, the reader is invited to read [Gal17a], where a characterization flow employing 3D EM simulations was developed and validated to accurately extract the Z_0 of transmission lines, excited using waveguide (modal) excitation. The scattering parameters computed during simulation are re-normalized to a given system value (i.e., $Z_{\mathrm{sys}} = 50\ \Omega$) and used in Equation (4.1) to compute the line characteristic impedance [Eis92]:

$$Z_0 = Z_{sys} \cdot \sqrt{\frac{(1 + S_{11}^2) - S_{21}^2}{(1 + S_{11}^2) - S_{21}^2}} \tag{4.1}$$

The approach was validated by benchmarking it with the calibration comparison method using a calibration kit integrated in the BEOL of the IHP SG13G2 130 nm SiGe BiCMOS technology. For the purposes of a fair comparison, the lines were designed to be uniform, with no line-to-pad discontinuities to provide an accurate test case for the calibration comparison method [Wil01]. The calibration kit was designed to allocate different waveguide bands from 75 GHz to 325 GHz. The micro-photographs of the WR-5 (140–220 GHz) structures are displayed in Figure 4.7(a–c), while Figure 4.7(d) shows the schematic line cross section.

The structures were simulated using three different 3D electro-magnetic simulators, Keysight EMPro, Ansoft HFSS, and CST Studio Suite, to check for simulation discrepancies. In the model, the meshed ground planes have been simplified considering a continuous metal connection, both vertically and horizontally. This simplification provides good approximation of the

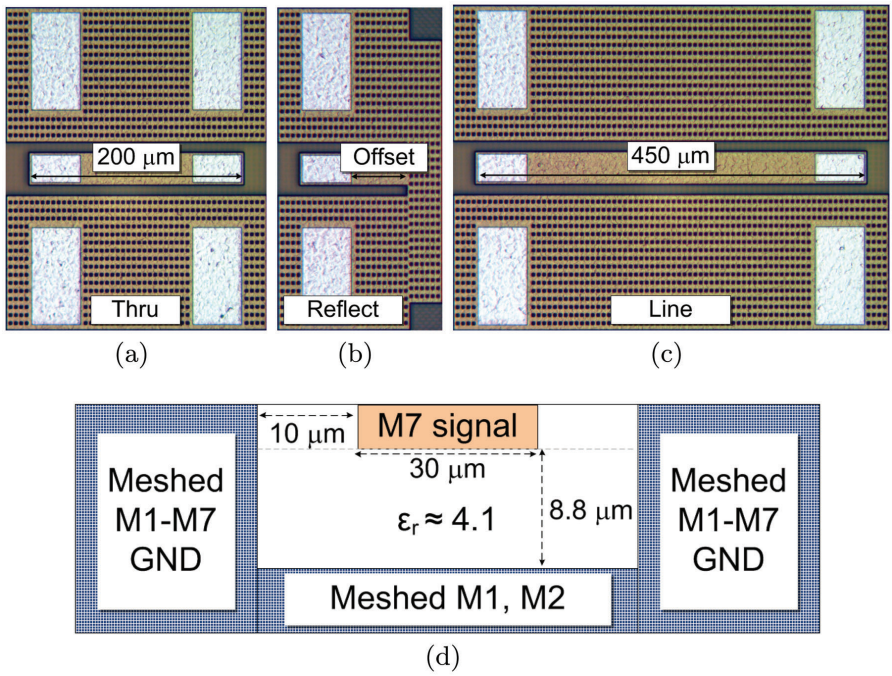
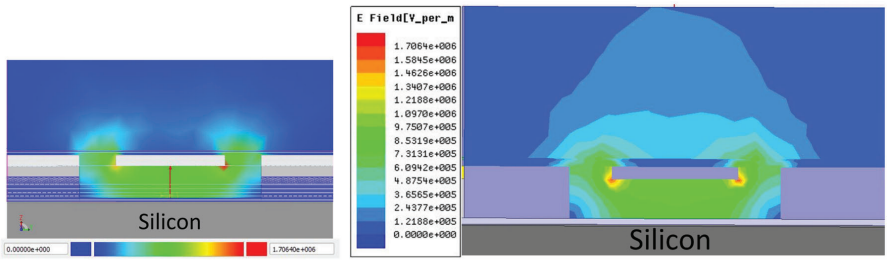


Figure 4.7 Coplanar wave guide CPW calibration structures realized on IHP SiGe 130 nm BiCMOS technology. (a) Microphotograph of the thru line, (b) of the reflect standard and (c) of the transmission line employed for the WR05 calibration kit, (d) schematic cross section of the CPW line.

electrical response of the structure since the openings in the metal mesh are much smaller than the wavelength (maximum aperture is in the order of $2.5 \times 2.5\ \mu m^2$). The excitation of the CPW lines is provided by means of waveguide (modal) ports. The simulator first solves a two-dimensional eigenvalue problem to find the waveguide modes of this port and then matches the fields on the port to the propagation mode pattern, and computes the generalized (i.e., mode matched) scattering parameters. In all the simulators, the port dimensions are designed using the rules of thumb described in [Wei08], ensuring ideally no fields at port boundaries, as also depicted in Figure 4.8 for two simulator examples.

Absorbing/radiation boundaries are then imposed at the lateral and top faces of the simulation box. The box is defined horizontally by the dimensions (length/width) of the simulated structure, and vertically by the wavelength ($\lambda/4$ at minimum simulation frequency). The bottom face of the simulation



(a) (b)

Figure 4.8 Field distribution on waveguide ports at 300 GHz when exciting the structures described in Figure 4.7, for (a) Keysight EMPro and (b) Ansoft HFSS.

box is defined as a perfect electric conductor, simulating the presence of a metallic chuck underneath the structure, as it is the case during measurements. The absorbing boundaries simulate an unperturbed propagation of the EM waves through this boundary. In this respect, the interference with other structures on the wafer is not taken into account in the simulation. Material parameters and lateral dimension are chosen according to the nominal technology values.

Figure 4.9 shows the comparison of the characteristic impedance computed using the proposed method (with different EM simulation tools), and the characteristic impedance extracted with measurements using the calibration comparison method [Wil01] and the Eisenstadt method [Eis92]. Both the measurement based methods are hampered by the (small) discontinuity presented by the probe to line transition, as predicted in [Mar92] and [Wil01]. The EM-based method offers fairly constant (with frequency) characteristic impedance response, as expected. It is interesting to note how simulations performed employing different EM tool, produce slightly different values for the characteristic impedance (max. 1 Ω for the real part and 0.1 Ω for the imaginary part), when applying similar settings in terms of meshing and solving methods. The differences can be attributed to different meshing algorithms, discretization, etc., of the tools which could all be categorized as the intrinsic uncertainty of the proposed method. This comparison shows how the proposed method provides comparable results to the state-of-the-art techniques, when the validity of the latter is still guaranteed by the transmission line design. As the method of [Gal17a] is ideally valid for any kind of transmission line, it can be employed also in situations in which large inductive probe-to-line transitions are present, which is the case when vias are involved.

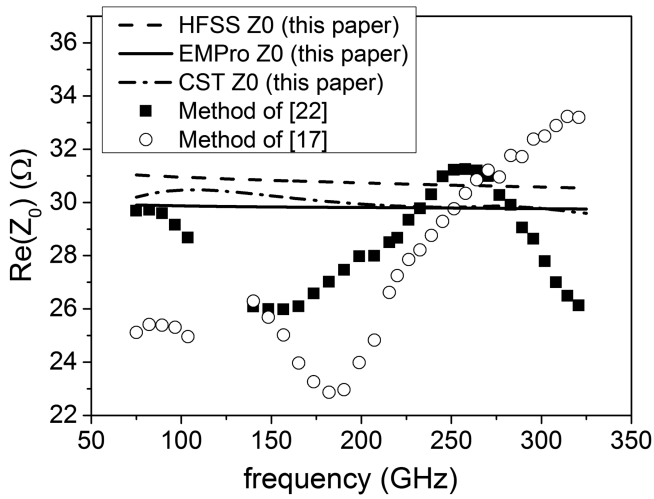


Figure 4.9 Real part of characteristic impedance for the line shown in Figure 4.7(a), computed with the simulation approach described in [Gal17a] (solid lines EMPro, dashed lines HFSS, dashed-dot lines CST), and measured using the method of [Eis92] (empty circles) and the method of [Wil91b] (filled squares).

In order to compare the different calibrations, the method of [Wil92] has been employed, defining an upper bound (UB) error metric as:

$$UB(f) = max\left|S'_{i,j}(f) - S_{i,j}(f)\right| \tag{4.2}$$

Where S' is the reference scattering matrix of the verification line (i.e., 3D simulated S-parameters), $S(f)$ is the frequency-dependent scattering matrix resulting from the investigated calibrations (i.e., LRM on alumina, TRL on fused silica and TRL on BiCMOS) and $i, j \in$ [1,2]. This metric defines the UB of the deviation of the S-parameters measured by one calibration and the reference S-parameters computed using EM simulations. The measurement data used to compute the error bound of Figure 4.10 are based on the same raw data of the verification line, thus removing any measurement variation of the verification structure from the error propagation mechanisms. On these raw data the respective calibration algorithm (with their respectively computed error terms) were applied. In addition, both the methods indicated as TRL on silicon in Figure 4.10 use also the same raw measurement in the calibration procedure (i.e., extraction of error terms), thus confining their difference only to the characteristic impedance values versus frequency, computed with the two different methods.

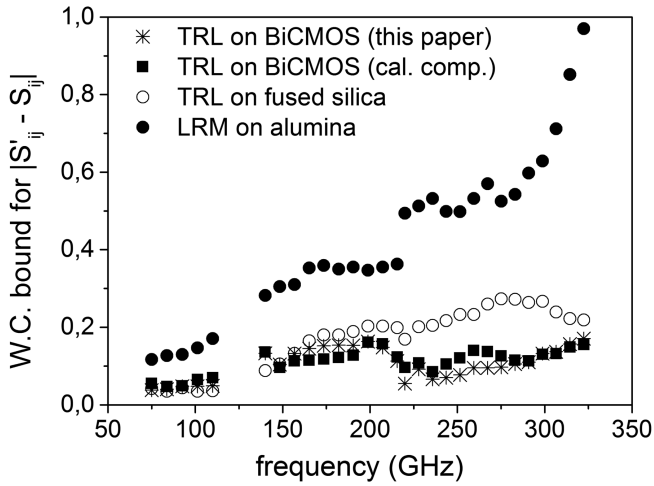


Figure 4.10 Comparison of probe-tips corrected measurements of a verification line manufactured on the SiGe BEOL in the frequency range 75–325 GHz for different calibrations.

As can be seen from Figure 4.10, the calibration performed on SiGe technology is the one that presents smaller deviation from the reference data, with an $UB \leq 0.17$ in the entire frequency band for both characteristic impedance extraction methods considered, i.e., the proposed EM-based method (Figure 4.10, asterisks) and the calibration comparison method (Figure 4.10, filled squares).

4.4 Direct DUT-plane Calibration

The method to derive the characteristic impedance of a transmission line described in the Section 4.3 "Direct On-wafer Calibration" will be applied to extract the Z_0 of transmission lines employed in a TRL calibration/ de-embedding kit to perform S-parameters measurements at the lowest metal layer (M1) for direct DUT access. Realizing transmission lines in the lowest metal layers can present several challenges, typically associated with the losses of the underlying substrate (i.e., conductive silicon). One solution was proposed in [Gal17b], where a CPW line realized at M1 was capacitively loaded with a series of floating metal bars (CL-ICPW), realized in a higher metal layer, in order to confine the propagating electromagnetic field in the low loss oxide of the BEOL.

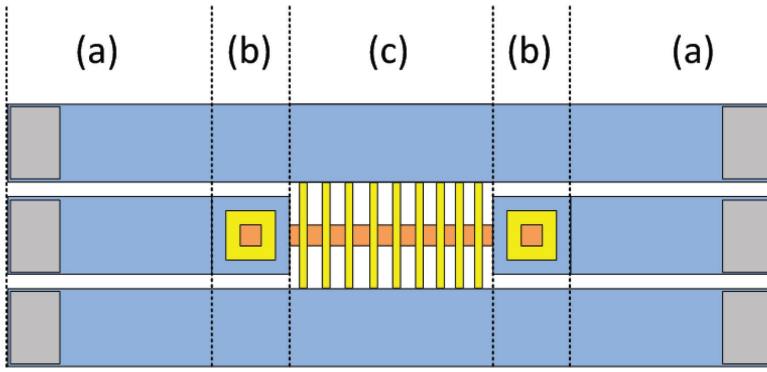


Figure 4.11 Simplified schematic top-view of a generic test-structure realized with CL-ICPW. (a) Input section, (b) M7-M1 vertical transition and (c) DUT stage.

This line topology can be employed in the TRL calibration/de-embedding kit, as depicted in Figure 4.11. The general structure of the fixture features three main sections: an input stage [pad plus launch line, section (a); a transition from top metal to M1, section (b), composed by all metal layers and interconnecting vias; and the final section (c), realized on M1 using CL-ICPWs that can feature a transmission line i.e., thru or line for the TRL de-embedding kit] or an offset short. The calibration/de-embedding kit, was manufactured using the BEOL of *Infineon's* 130 nm SiGe BiCMOS technology B11HFC, featuring seven metal layers. Figure 4.12(a) shows a cross section of Figure 4.11, section (a), where M3 is used as ground shield in order to isolate the CPW from the lossy substrate. The transition from the top metal center conductor of the CPW to the M1 center conductor of the CL-ICPW is realized using a gradual, inverse pyramidal shape. This allows to connect the large top metal conductor (i.e., 30 μm width) with the smaller M1 line, keeping the ground reference at the same metal level (i.e., M3) as shown in Figure 4.12(b).

For the DUT stage, M3 is chosen as the metal layer for the floating shield. This choice allows reducing the losses while guaranteeing a Z_0 of 34 Ω, sufficiently close to the 50 Ω required to minimize the errors arising from reflection losses when measuring in a conventional VNA-based setup [Mub15]. The shield is realized with 2 μm wide metal strips and a fill factor of 50% in order to respect the density rules. The cross section of the final design for the CL-ICPW is shown in Figure 4.12(c). Micro-photographs of the calibration/de-embedding kit for WR-3 (220–325 GHz) waveguide bandwidth are shown in Figure 4.13.

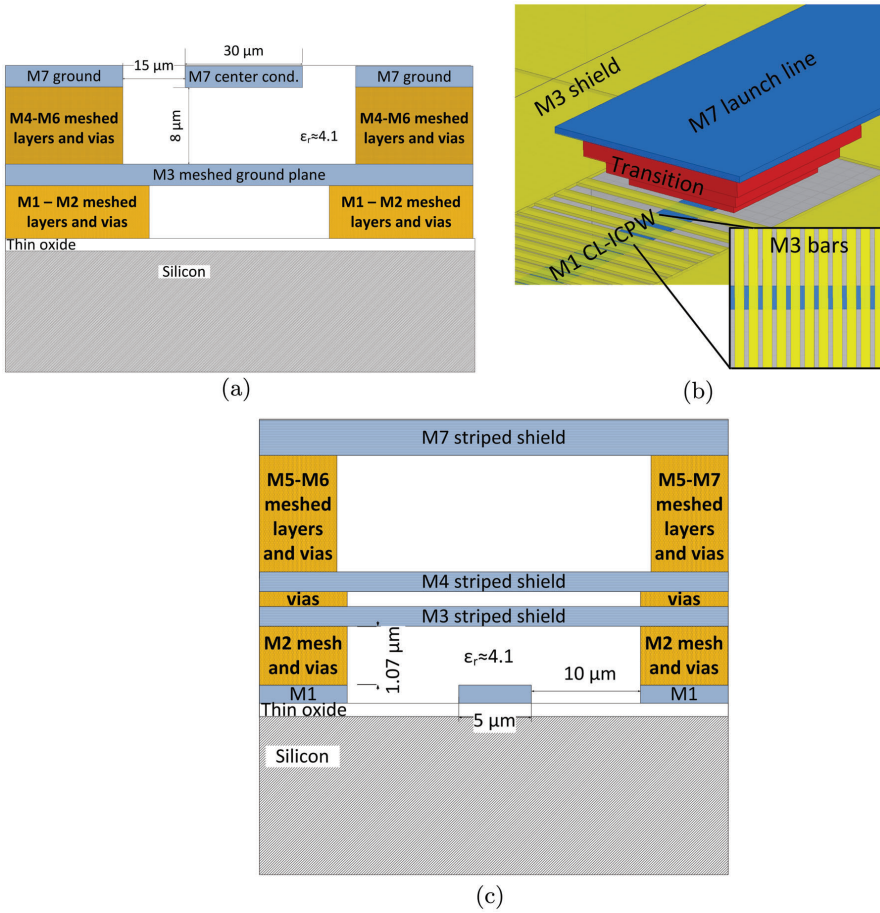


Figure 4.12 Schematic cross section of the input stage used for the test structures (a). 3D model of the vertical transition connecting the central conductor of the input stage in M7 to the CL-ICPW central conductor in M1 (b). Schematic cross section of the CL-ICPW employed in the DUT stage of the calibration kit (c).

The kit employs 130 µm long launch lines. The thru standard is realized by means of a 150 µm CL-ICPW, and it is designed to embed the final DUT (transistor here) in its center reference plane. The de-embedding kit reflects are realized by two symmetric offset shorts, with an offset equal to half the thru length. Further, a longer line with an additional 80 µm length for the CL-ICPW, in respect to the thru, is realized as the line standard. Finally, a test structure consisting of a 310 µm long CL-ICPW has been realized for

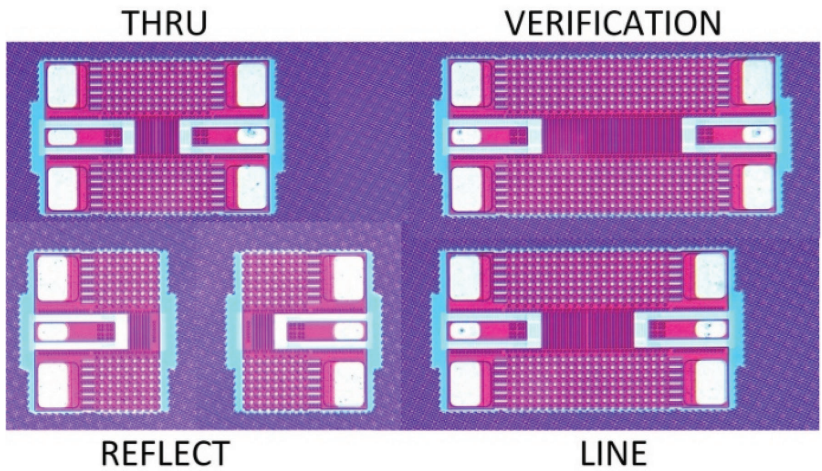


Figure 4.13 Micrograph of the de-embedding kit on Infineon B11HFC technology.

verification. EM simulations are then performed to extract the characteristic impedance of the line. Note that the only structures simulated are the CL-ICPW in Figure 4.12, section (c). For this purpose, the procedure described in Section 4.2 is employed. Once the characteristic impedance is extracted, the proposed kit can be employed for direct calibration at M1. To demonstrate the proposed calibration/de-embedding method in its final application, measurements of a heterojunction bipolar transistor (HBT) featuring two emitter fingers with 5 μm length and 220 nm width were performed. The device was embedded into the test fixture employing CL-ICPW in common-emitter (CE) configuration directly at the calibration reference planes, shown in Figure 4.14. To guarantee proper connection between the CL-ICPW test structure and the transistor (BECEB) modeled in the process design kit (PDK) (i.e., employing a p-type guard ring around the active device, with ground contacts connected to metal level 1) a small bridge at metal 2 (see, Figure 4.14(b) was added. After calibration, EM simulations of these lines are used to de-embed them from the measurements. Note, that the configuration and interconnections (no M1 connections between the emitters and the bases) is only illustrative of the technique. When a different reference plane needs to be defined and different parasitic element included or excluded from the device model this can be achieved by properly setting the reference plane of the calibration through the proper design of the reflect standard and the zero length thru position.

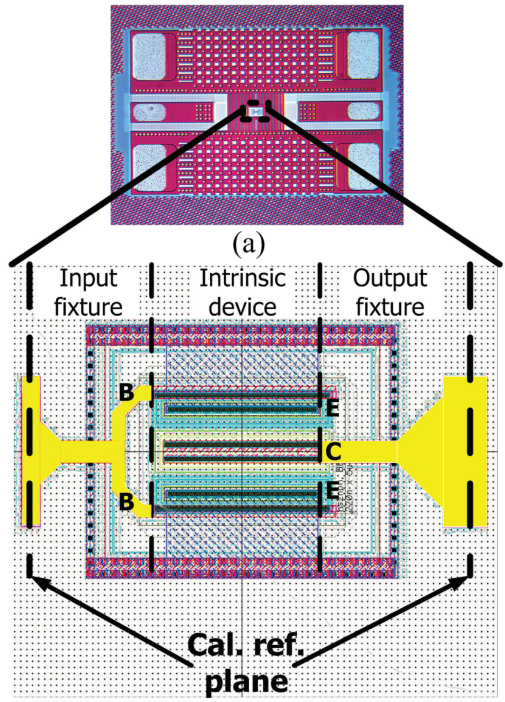


Figure 4.14 Top view of the transistor (BECEB) integrated into the test-structure (a) Detailed view of the layout for the integrated transistor (b), highlighting the input and output fixture (in yellow) required to guarantee connection to the intrinsic device. The base, collector, and emitter contact (B, C, and E, respectively) are marked on the layout.

The device S-parameters have been measured using the direct calibration technique in the frequency range from 220 to 325 GHz, using fixed bias conditions ensuring close to peak f_{T}, i.e., V_{CE} = 1.5 V and V_{BE} = 0.91 V. The measurement results are then compared with the S-parameters obtained by using the HICUM level 2 model of the device. The device selected in the layout of this work was not supported by a model in the PDK so that an approximate set of parameters had to be generated. Figure 4.15(a) shows the comparison of the magnitude in dB for all the S-parameters of the considered transistor. The measured values for S_{11} and S_{21} agree quite well with the model prediction, with discrepancies in the order of 0.2 dB, while S_{22} shows a bigger error, with a maximum value in the order of 1.1 dB in the entire frequency range. The S_{12} parameter shows the biggest relative

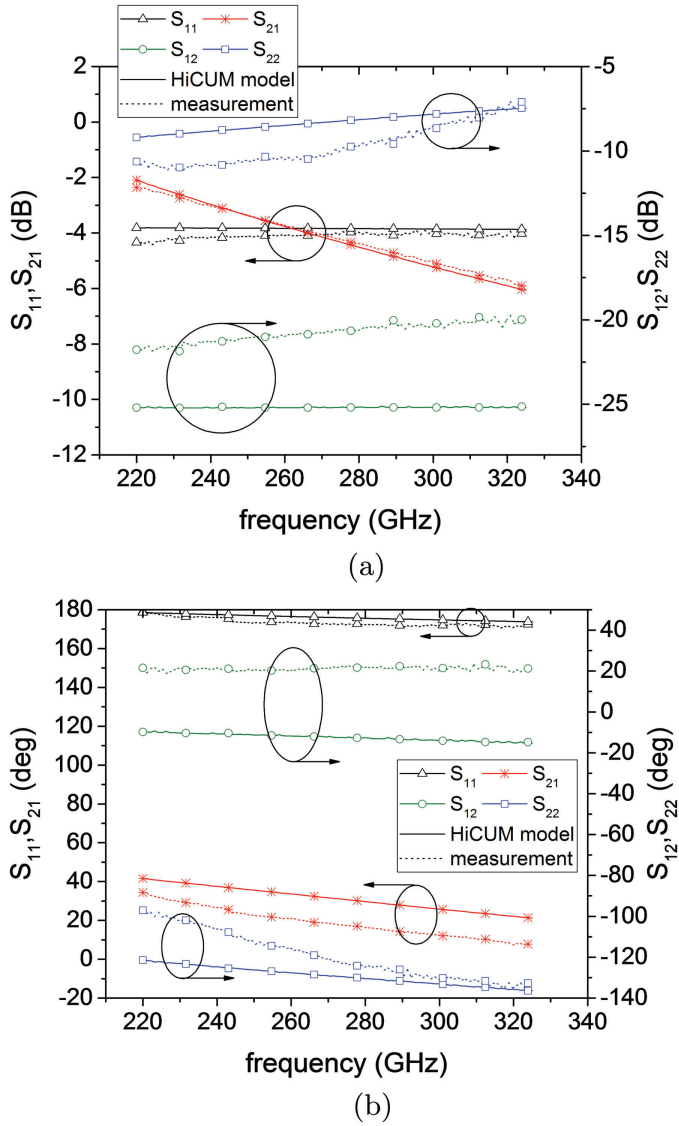


Figure 4.15 S-parameter measurements (dotted lines) versus model of the considered Infineon transistor (solid lines) for both a) Amplitude (in dB) and b) Phase (in degrees).

error in magnitude, due to its small absolute value. Discrepancies between measurements and model are more significant when considering the phase information (see, Figure 4.15(b)) where they can reach 40 degrees for S_{12}.

4.5 Conclusion

In this chapter various concepts and techniques to achieve accurate calibration techniques at (sub)mm-waves for device characterization have been reviewed. The problems of electrically thick substrates have been explained and experimentally validated. Electrically thin substrates with their performance improvement were discussed. The problems and possible error compensations related to substrate transfers are addressed. A complete flow and an EM-based technique to design and characterize TRL-based calibration kits to be embedded in the BEOL of commercial silicon technologies were described. Finally, an approach to realize direct calibration/de-embedding kits capable of measuring the device performance at M1 was presented and experimentally validated.

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