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## SiGe HBT Compact Modeling

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A. Pawlak<sup>1</sup>, M. Schröter<sup>1,2</sup> and B. Ardouin<sup>3</sup>

<sup>1</sup>Chair for Electron Devices and Integrated Circuits, Technische Universität Dresden, Germany

<sup>2</sup>Department of Electrical and Computer Engineering, University of California at San Diego, USA

<sup>3</sup>XMOD Technologies, France

### Abstract

Fabrication and circuit design are linked by compact device modeling; i.e., the electrical characteristics of the devices fabricated on a wafer are represented by sufficiently simple but preferably still physics-based models that are suitable for circuit simulation and optimization. The importance of modeling has been growing rapidly due to strongly increased device complexity, manufacturing cost, and fabrication time. There is an increased demand from industry for first-pass success of high-frequency (HF) analog circuits in order to stay competitive. For SiGeC HBT technologies, ranging from production to the most advanced process, this has been successfully addressed by the standard compact bipolar transistor model HICUM/L2 [Schr10].

For practical applications, a compact model (CM) itself is not sufficient though. Its model parameters need to be determined from measurements of terminal (current, voltage) characteristics, preferably making use of clever test structures and mathematical manipulations (so-called parameter extraction methods) in order to be able to separate the various, often superimposed, physical effects and their related parameters. Consistent physics-based parameter extraction methods that provide for a given process accurate geometry-scalable and statistical device models not only represent a key enabler to first-pass design success but also yield important information for process development. One objective of DOTSEVEN was the development of

improved or even new parameter extraction methods and to provide a unified set of test structures.

### 3.1 Introduction

The predicted THz performance of SiGeC HBTs along with their integration with digital CMOS indicates a bright future of the corresponding BiCMOS technologies for serving HF applications [Sch11a, Sch11b, Sch16a]. These predictions and the rising demand for mm- and sub-mm-wave<sup>1</sup> applications have motivated the development of improved SiGeC process technologies, leading to the most recent results [Hei16] of  $(f_T, f_{\max}) = (505, 720)$  GHz fabricated with a 130 nm lithography within the DOTSEVEN project.

The large variety of HF applications requires a versatile and accurate representation of such process technologies within the design kits in order to enable circuit optimization and exploiting the performance limits of the technology. Thus, an important focus of DOTSEVEN was the development of suitable simulation and modeling tools as well as the verification of the new models [Sch16c]. The corresponding effort on compact modeling of high-speed SiGeC HBTs and the associated experimental results are presented in this chapter.

Compact models – which are also sometimes called *electrical models* or *SPICE models* – were introduced in the 1970s as a constitutive and inseparable part of simulators for electronic circuits. Based on a set of parameterized analytical equations, CMs are meant to provide a suitable representation of the electrical characteristics of electronic devices under given bias, frequency, and temperature conditions. The large variety of applications in the Si industry has led to a strong preference for physics-based CMs, in which (i) the formulations for current and charge are derived as simplified solutions of fundamental equations for carrier transport and electrostatics, (ii) most of the parameters retain a physical meaning, and (iii) the equivalent circuit corresponds to the physical structure of the device. Such physics-based models enable not only device sizing-based circuit optimization but also efficient modeling of statistical process variations and process debugging.

The determination of the model parameters from device measurements, typically called *parameter extraction*, includes the specification of measurement conditions and the mathematical procedure for data manipulation for obtaining the desired parameter values. This task is sometimes, especially in

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<sup>1</sup>In this chapter, the designation HF will be used for all these frequency ranges.

the III–V community, called model extraction. This incorrectly implies the “construction” of the CM, which is actually not included. Similarly, often just the term *model* is used referring to both the CM (formulation) and its associated parameter set. Since for the vast majority of application cases the CM is given, the usually tedious and lengthy task of its development should be distinguished from the task of extracting its parameters.

While CMs are developed independently of circuit simulators, the availability of high-level description languages (such as Verilog-A, cf. e.g., [Muk16]) and associated model compilers has significantly sped up not only the model implementation but also its release for all commercial simulators in the form of a single (reference) model code.

The various tasks mentioned above eventually lead to a working CM. When evaluating its accuracy, different aspects come into play, which are sometimes a source of confusion. The necessary conditions for obtaining an accurate CM are listed below:

1. The intrinsic ability of a CM to describe a device, i.e., the versatility and accuracy of its constitutive equations and its equivalent circuit.
2. The model coding by its developers (e.g., in Verilog-A), e.g., correctly modeling capacitances by their respective charges, following from the integration of the capacitance between equilibrium and the controlling voltage(s).
3. A correct model implementation by the EDA vendors in their circuit simulator. Even when using appropriate tools, like model compilers, this step induces many non-trivial optimizations and customizations, which can be a source of error.
4. The accuracy of the model parameters, i.e., how accurate the individual electrical characteristics of the model agree with those of the measured device to be represented.

Only meeting all of the above criteria with sufficient quality will provide the desired CM accuracy for a given technology or process. No matter how accurate and versatile the CM itself may be, poorly determined parameters will ruin the effort spent not only on its development but also for process development and circuit design.

Compact modeling of high-speed SiGeC HBTs within DOTSEVEN addressed two main aspects. First, libraries with geometry scalable model parameters for the HBTs fabricated in the project were provided, enabling the design of mm-wave circuit building blocks and demonstrators. Second, CMs in combination with TCAD were employed for analyzing the process in terms of causes of performance reduction by separating 3D parasitic

effects from 1D transport effects in the intrinsic device structure [Kor15]. The compact HBT modeling in the project was based on HICUM Level 2 (L2), which has been a CMC supported standard since 2004. Compared to other existing CMs, HICUM/L2 has been continuously developed for HF/high-speed HBT technologies and applications and offers various HF-specific features as well as high accuracy up to higher frequencies and over a wider bias range. This chapter highlights recent model extensions that are relevant for DOTSEVEN-like technologies. Furthermore, important steps during parameter extraction are presented with an emphasis on the model extensions and physics-based geometry scaling. In addition, most recent evaluations of methods for determining the series resistances are briefly discussed.

Section 3.7 gives an overview about publications showing comparisons of DC, AC and non-linear large-signal characteristics with experimental data.

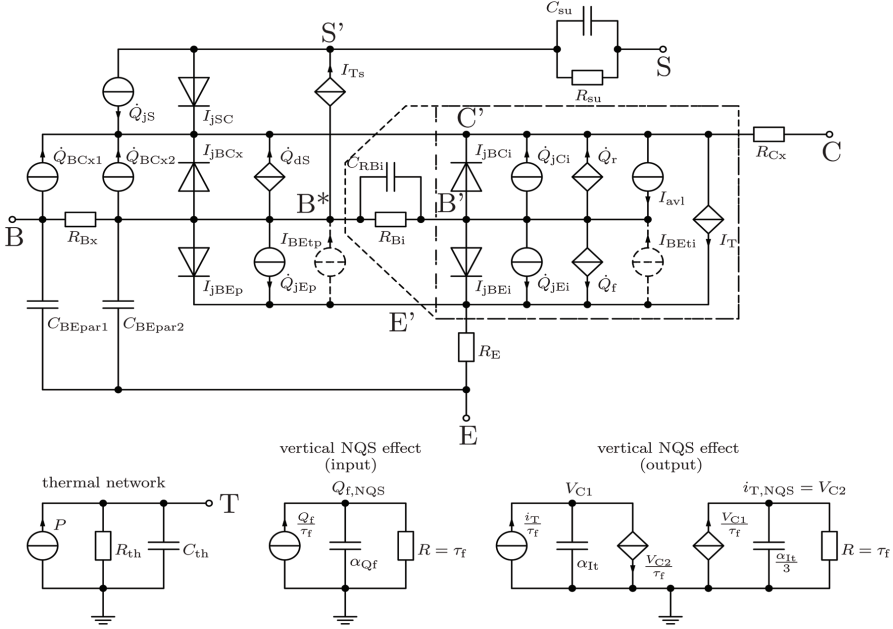
### 3.2 Overview of HICUM Level 2

A detailed derivation of the formulations of HICUM/L2 can be found in [Sch10] and is beyond the scope of this book. Below, just a brief overview of the model components is given to provide a reference for further discussions.

The equivalent circuit of HICUM/L2 is displayed in Figure 3.1. The intrinsic (1D) transistor behavior is described by the controlled current source for the transfer current  $I_T$ , that is calculated based on the generalized integral charge-control relation (GICCR, cf. Section 3.3), the dynamic currents resulting from the time-dependent depletion charges ( $Q_{jEi}$ ,  $Q_{jCi}$ ) and diffusion charges ( $Q_{dEi}$ ,  $Q_{dCi}$ ), and diodes for the currents injected into the emitter ( $I_{jBEi}$ ) and collector ( $I_{jBCi}$ ). Collector impact ionization is represented by the current  $I_{avl}$ . As proved in [Sch16b], the complicated behavior of the (ohmic) intrinsic collector (epi) region can be accurately described within the GICCR framework and does not require a separate element with a typically complicated description as it is the case in some other CMs.

Laterally distributed effects in the internal base region are modeled by the bias-dependent internal base resistance  $R_{Bi}$ , which takes conductivity modulation and emitter current crowding into account. Dynamic emitter current crowding during small-signal operation is modeled by the parallel capacitance  $C_{RBi}$ .

The injection across the emitter perimeter junction is represented by  $Q_{jEp}$  and  $I_{jBEp}$ . The current source  $I_{BET(i,p)}$  models band-to-band (BTB) tunneling and can be connected either to the internal (B') or to the perimeter (B\*) base node, depending on the transistor architecture.



**Figure 3.1** Equivalent circuit of HICUM/L2 including the adjunct networks for modeling electro-thermal effects and NQS effects. Not shown are the networks for modeling correlated noise [Her12, Sak15, Sch10]. The dash-dotted line defines the intrinsic (1D) transistor representation and the dashed line defines the internal transistor.

The external BC region is modeled by the junction current  $I_{jBCx}$  and the dynamic currents through the time-dependent charges  $Q_{jC'x}$  and  $Q_{jC''x}$ . The latter include the depletion charge in the external base as well as the oxide capacitance of the shallow trench and contact region related parasitic capacitance between the base and the collector. The charges are split across the external base resistance to account for distributed lateral effects at high frequencies. The emitter contact and poly-silicon resistance are represented by  $R_E$ , while the external collector resistance  $R_{Cx}$  includes the collector contact, sinker, and buried layer contributions. The capacitances  $C_{BE,par1}$  and  $C_{BE,par2}$  include the BE spacer and parasitic poly-silicon contact region related capacitances between the base and the emitter.

The substrate transistor is modeled with simple expressions for the transfer current source  $I_{Ts}$  and the respective back-injection current  $I_{jSC}$ . The SC depletion charge is modeled by  $Q_{jS}$ , and a simple bias-independent storage time is used for describing the diffusion charge  $Q_{dS}$ .

Substrate coupling effects are described by a simple first-order frequency dependence with  $R_{\text{Su}}$  representing the finite resistance of the path between sub-collector and substrate contact and  $C_{\text{Su}}$  caused by the permittivity of the bulk substrate. An improvement of this simple equivalent circuit is presented in Section 3.5. Note that, based on the final circuit layout, any elaborate equivalent circuit can be connected to the substrate node.

Electro-thermal effects are taken into account by a simple first-order low-pass network consisting of the thermal resistance  $R_{\text{th}}$  and thermal capacitance  $C_{\text{th}}$ . The externally available temperature node allows the connection of both higher order and thermal coupling networks if required by the application [Leh14].

The extraordinary performance of SiGeC HBTs in DOTSEVEN has been achieved with changes in the transistor architecture. Changes in lateral directions result in a modification of both geometry scaling laws and the equivalent circuit. The most relevant aspects here will be discussed in Sections 3.5 and 3.6.3. Structural changes in the vertical direction impact the intrinsic transistor behavior. They have been accounted for in the formulations for the transfer current and stored charge, which will be discussed in the next two chapters. In versions of HICUM/L2 previous to 2.3, those effects were not considered explicitly, which led to increased effort for parameter extraction using conventional methods, potentially yielding non-physical model parameters.

### 3.3 Modeling of the Quasi-Static Transfer Current

#### 3.3.1 Basics of the GICCR

As shown in [Sch10, Sch16b], the GICCR can be derived as closed-form solution from integrating the 3D drift-diffusion transport equation. This section summarizes the relevant features of the GICCR by focusing on just the vertical (1D) npn transistor structure. In this case, the 1D GICCR master equation reads

$$I_T = \frac{(qA_E)^2 V_T \overline{\mu_{nB} n_{iB}^2}}{Q_{\text{ph}}} \left[ \exp\left(\frac{V_{B'E'}}{V_T}\right) - \exp\left(\frac{V_{B'C'}}{V_T}\right) \right] = I_{\text{Tf}} - I_{\text{Tr}}, \quad (3.1)$$

with the elementary charge  $q$ , the emitter area  $A_E$ , the thermal voltage  $V_T$ , the electron mobility  $\mu_n$ , the intrinsic carrier density  $n_i$ , and the voltages between the terminals of the 1D transistor  $V_{B'E'}$  and  $V_{B'C'}$ . The denominator results

$$Q_{\text{ph}} = A_E q \int_{x'_E}^{x_{C'}} h(x) p(x) dx \quad (3.2)$$

from integrating the transport equation from the mono- to poly-silicon emitter interface, which defines the 1D emitter contact  $x_{E'}$ , to the peak of the buried layer, which defines the 1D collector contact  $x_{C'}$ .  $Q_{\text{ph}}$  is a weighted hole charge, with  $p$  being the hole carrier density and the weight function  $h(x)$

$$h(x) = h_g(x) h_J(x) h_v(x). \quad (3.3)$$

Its first component,

$$h_g(x) = \frac{\overline{\mu_{\text{nB}} n_{\text{iB}}^2}}{\mu_{\text{n}}(x) n_{\text{i}}^2(x)}, \quad (3.4)$$

accounts for all effects related to the field-dependent electron mobility and the spatially varying bandgap. The normalization factor  $\overline{\mu_{\text{nB}} n_{\text{iB}}^2}$  is taken as average value over the neutral base. The second component,

$$h_J(x) = -\frac{A_E J_n(x)}{I_T}, \quad (3.5)$$

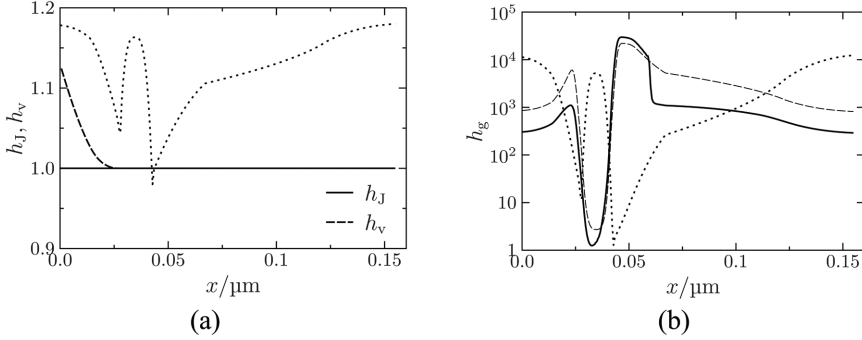
is, in the 1D case, related to volume recombination, while in the 3D case it also accounts for the lateral spreading of electron current density, typically in the collector. The third term

$$h_v(x) = \exp\left(\frac{V_{B'E'} - \varphi_p(x)}{V_T}\right), \quad (3.6)$$

takes into account the spatial variation of the hole Fermi-potential  $\varphi_p$  w.r.t. the chosen controlling (node) voltage. The deviation is expected to be negligible across the vertical neutral base region, but can become significant in the 3D case for emitter current crowding.

The spatial dependence of the components (3.4) and (3.5) in Figure 3.2(a) shows that  $h_J$  and  $h_v$  are close to 1 in those regions where the hole density matters.

In contrast, the weight function  $h_g$  shown in Figure 3.2(b) follows mostly the spatial dependence of the bandgap, except for the BC depletion region, where both mobility and hole density are much lower than in the other transistor regions. As a consequence, for the  $i_T$  formulation of the intrinsic transistor only the impact of  $h_g$  and, in particular, of the bandgap needs to be taken into account. The influence of  $h_J$  and  $h_v$  can be included in the



**Figure 3.2** Spatial dependence of the weight functions (a)  $h_J$  and  $h_v$  for  $J_C = 5\text{mA}/\mu\text{m}^2$ , and (b)  $h_g$  (solid line) for low injection. In both pictures the dotted line shows the 1D doping profile in log-scale. In (b), the dashed line shows the bandgap in linear scale.

3D formulation through the weighted charge formulation (collector current spreading) and the internal base resistance (emitter current crowding).

For compact modeling, it is useful to split  $Q_{\text{ph}}$  into several components according to the device structure and transistor operation principle. The most suitable split leads to the sum of a zero-bias hole charge  $Q_{\text{p0}}$  and an excess charge  $\Delta Q_{\text{ph}}$  given by the change  $\Delta p$  of the hole density with non-zero bias:

$$\Delta Q_{\text{ph}} = q \int_{x_{\text{E}'} }^{x_{\text{C}'}} h(x) \Delta p(x) dx = h_{\text{jEi}} Q_{\text{jEi}} + h_{\text{jCi}} Q_{\text{jCi}} + Q_{\text{fh}}. \quad (3.7)$$

Here,  $Q_{\text{jEi}}$  and  $Q_{\text{jCi}}$  are the physical depletion charges of both junctions with the corresponding weight factors  $h_{\text{jEi}}$  and  $h_{\text{jCi}}$ , and  $Q_{\text{fh}}$  is the weighted mobile charge in the transistor. The normalization factor  $\overline{\mu_{\text{nB}} n_{\text{iB}}^2}$  in  $h_g$  and (3.1) is chosen such that the weight factor for  $Q_{\text{p0}}$  becomes 1. The other weight factors in (3.7) are defined as average values in the corresponding transistor region  $k$ :

$$h_k = \frac{\int_k h(x) \Delta p(x) dx}{\int_k \Delta p(x) dx} = \frac{q \int_k h(x) \Delta p(x) dx}{Q_k}. \quad (3.8)$$

The weighted mobile hole charge in (3.7) is further divided according to the different transistor regions:

$$Q_{\text{fh}} = h_{\text{f0}} \tau_{\text{f0}} I_{\text{Tf}} + h_{\text{fE}} \Delta Q_{\text{fE}} + \Delta Q_{\text{fB}} + h_{\text{fC}} Q_{\text{fC}} + \tau_{\text{r}} I_{\text{Tr}}. \quad (3.9)$$

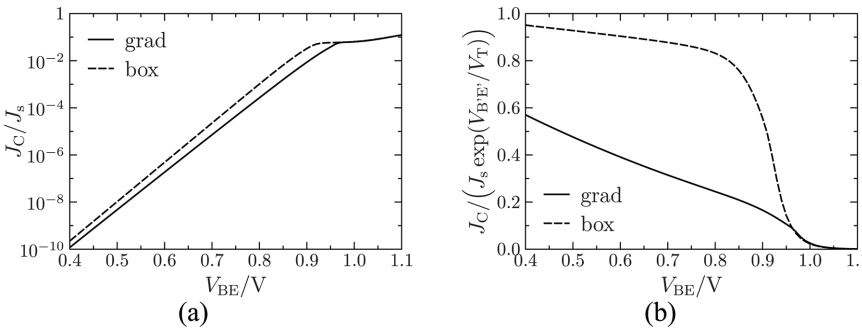
Here,  $I_{\text{Tf}}$  and  $I_{\text{Tr}}$  are the forward and reverse transfer currents, respectively, as defined in (3.1), with  $\tau_{\text{f0}}$ , and  $\tau_{\text{r}}$  being the corresponding (low current)

transit times.  $\Delta Q_{\text{fE}}$ ,  $\Delta Q_{\text{fB}}$ , and  $Q_{\text{fC}}$  are the physically stored excess charges in the emitter, base and collector regions at medium and high current densities at forward operation, while  $h_{\text{f0}}$ ,  $h_{\text{fE}}$ , and  $h_{\text{fC}}$  are the corresponding weight factors according to (3.8). The weight factor for the base charge is left close to 1 since the value of  $h_{\text{g}}$  is close to 1 (cf. Figure 3.2(b)) due to the choice of  $\overline{\mu_{\text{nB}} n_{\text{iB}}}$ . To keep the model simple. Also no dedicated weight factor is used for the reverse charge. Note that although  $Q_{\text{ph}}$  is related to the actual hole charge, it does not have a physical representation by itself in the transistor. Thus, in contrast to the actual charge, it cannot be measured directly.

In summary, the GICCR in the form of (3.1) represents a physically consistent closed-form description for the transfer current of HBTs, which also provides clear guidance on how additional effects need to be included. The following sections describe the extensions of the GICCR presented above with respect to the advanced SiGe HBT technology developed in DOTSEVEN and related projects (DOTFIVE, RF2THz).

### 3.3.2 SiGe HBT Extensions

Within DOTFIVE and DOTSEVEN very different approaches toward SiGe HBT technology development were taken. When investigating the fabricated HBTs, significant differences in the ideality of the transfer current characteristic and in the current density dependence of the corresponding transconductance had been observed. An example of this behavior is shown in Figure 3.3(a). The observed differences were eventually traced back to different Ge profiles in these technologies, in particular within the BE



**Figure 3.3** (a) Transfer current for transistors with different Ge profiles in the base. (b) Transfer current normalized to their ideal formulation for the same transistors as in (a) at room temperature and  $V_{\text{B'C'}} = 0$  V.

space-charge region (SCR), cf. [Paw14a]. While spatially constant Ge profiles show the expected almost ideal behavior, grading the Ge already within the BE SCR led to a significant deterioration in ideality and the transconductance already at medium collector current densities.

Normalizing the transfer current to its ideal form,  $I_s \exp(V_{BE}/V_T)$ , magnifies the above mentioned non-ideality as shown in Figure 3.3(b). This increase in non-ideality was first noted in [Cra93] and later modeled in [Paa01] by modifying the Gummel number. In this section, the origin of the effect will be briefly reviewed and then its incorporation into the transfer current expression by applying the GICCR will be demonstrated.

A graded Ge profile leads to a spatially dependent bandgap in the base region which in turn leads to a spatially dependent intrinsic carrier density

$$n_i(x) = n_{i0} \exp\left(\frac{\Delta V_g(x)}{2V_T}\right) \quad (3.10)$$

with  $n_{i0}$  representing pure Si and  $\Delta V_g(> 0)$  as the bandgap reduction due to the Ge mole fraction. Since the bandgap decreased with increasing Ge content, the intrinsic carrier density increases with  $x$ .

According to the classical theory for bipolar transistors, the electron density  $n_e$  injected at the beginning  $x_e$  of the neutral base (cf. Figure 3.4) is given by:

$$n_e = \frac{n_i^2(x_e)}{N_B} \exp\left(\frac{V_{B'E'}}{V_T}\right). \quad (3.11)$$

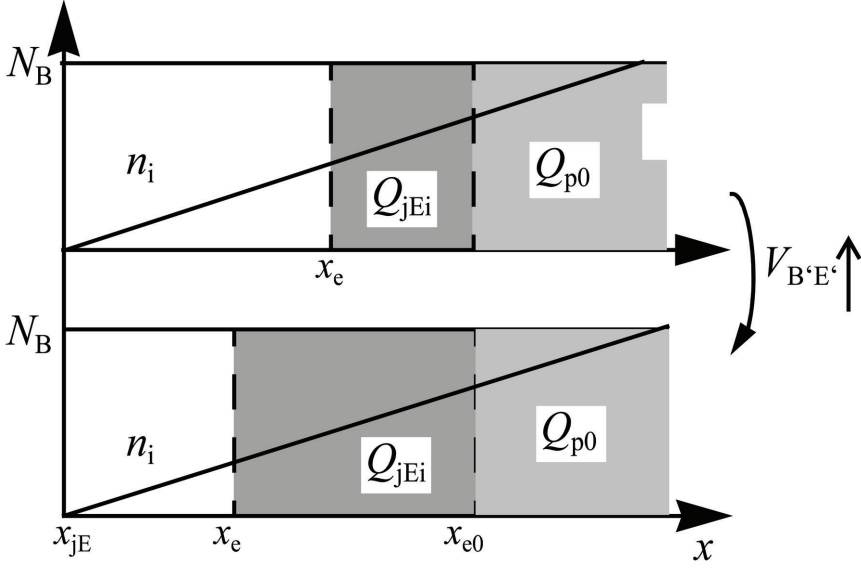
With increasing forward voltage  $V_{B'E'}$  across the BE SCR,  $x_e$  moves towards the junction and thus smaller values of  $n_i$ . This in turn reduces the injected electron density compared to the ideal case of a spatially independent  $n_i$  and leads to the non-ideality observed in Figure 3.4.<sup>2</sup>

The varying  $n_i$  enters the GICCR via the weight function (3.4), which needs to be inserted into (3.7) in order to calculate the weight factor  $h_{jEi}$  for  $Q_{jEi}$ . In the following derivation, a spatially constant base doping profile is assumed for  $x_{jE} < x \leq x_{e0}$ . Also, for simplifying the expressions, a coordinate transformation is applied such that  $x_{jE}$  is chosen as new reference:

$$x' = x - x_{jE}. \quad (3.12)$$

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<sup>2</sup>Note that from Figure 3.4 the depletion charge follows as  $Q_{jEi} = qN_B(x_{e0} - x_e)$ .



**Figure 3.4** Visualization of the depletion charge in the base–emitter space charge region for two bias points with increasing voltage from the top picture to the bottom. The intrinsic carrier density is given in log-scale.  $x_{jE}$  relates to the metallurgic BE junction, while  $x_e$  and  $x_{e0}$ , respectively, are the boundaries of the space charge region for  $V_{B'E'} > 0V$  and  $V_{B'E'} = 0V$ , respectively.

Assuming a fully depleted SCR, i.e.,  $p = 0$  for  $x_{jE} \leq x < x_e$ , and  $p = N_B$  in  $x_e \leq x < x_{e0}$ , the weight factor is given by:

$$h_{jEi} = \frac{\int_{x'_{e0}}^{x'_e} h(x') \Delta p(x') dx'}{\int_{x'_{e0}}^{x'_e} \Delta p(x') dx'} = \frac{N_B \int_{x'_{e0}}^{x'_e} h(x') dx'}{N_B (x'_e - x'_{e0})} = \frac{\int_{x'_{e0}}^{x'_e} h(x') dx'}{x'_e - x'_{e0}}. \quad (3.13)$$

Inserting (3.4) with (3.10) and assuming a spatially independent electron mobility yields:

$$h_{jEi} = \frac{\frac{\mu_{nB} n_{iB}^2}{\mu_n n_{i,jE}} \int_{x_{e0}}^{x_e} \exp\left(-\frac{\Delta V_g(x)}{V_T}\right) dx}{x'_e - x'_{e0}} = \frac{c_{hBE} \int_{x'_{e0}}^{x'_e} \exp\left(-\frac{\Delta V_g(x)}{V_T}\right) dx}{x'_e - x'_{e0}} \quad (3.14)$$

with  $n_{i,jE} = n_i(x_{jE})$ . The spatially linear bandgap variation is given by:

$$\Delta V_g(x) = \frac{\Delta V_{g,max} x'}{V_T x'_{Vg,max}} = \frac{x'}{a_{ni}}, \quad (3.15)$$

with the maximum bandgap change  $\Delta V_{g,\max}$  and the location of this maximum,  $x'_{V_{g,\max}}$ . Inserting this into (3.14) leads to

$$h_{jEi} = -a_{ni}c_{hBE} \frac{\exp\left(-\frac{x'_e}{a_{ni}}\right) - \exp\left(-\frac{x'_{e0}}{a_{ni}}\right)}{x'_e - x'_{e0}}. \quad (3.16)$$

Following classical theory, the width of the SCR is

$$x'_e = x'_{e0} \sqrt{1 - \frac{V_{B'E'}}{V_{DEi}}}, \quad (3.17)$$

which finally leads to

$$h_{jEi} = c_{hBE} \exp\left(-\frac{x'_{e0}}{a_{ni}}\right) \frac{\exp\left(\frac{x'_{e0}}{a_{ni}} \left(1 - \sqrt{1 - \frac{V_{B'E'}}{V_{DEi}}}\right)\right) - 1}{\frac{x'_{e0}}{a_{ni}} \left(1 - \sqrt{1 - \frac{V_{B'E'}}{V_{DEi}}}\right)}. \quad (3.18)$$

A similar expression can also be obtained for an exponential dependence of the base doping profile within  $x_{jE} \leq x < x_{e0}$ .

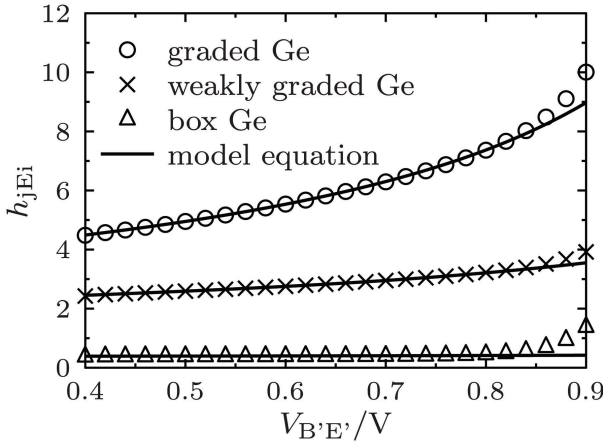
Replacing the square root by the grading coefficient  $z_{Ei}$ , which allows to capture realistic base doping profile shapes, yields the final model equation

$$h_{jEi} = h_{jEi0} \frac{\exp\left(a_{hjEi} \left(1 - \left(-1 \frac{V_{B'E'}}{V_{DEi}}\right)^{z_{Ei}}\right)\right) - 1}{a_{hjEi} \left(1 - \left(-1 \frac{V_{B'E'}}{V_{DEi}}\right)^{z_{Ei}}\right)} \quad (3.19)$$

where various quantities in (3.18) have been merged into the model parameters  $a_{hjEi} = x'_{e0}/a_{ni}$  and  $h_{jEi0} = c_{hBE} \exp(-a_{hjEi})$ .

The application of the model is shown in Figure 3.5 for transistors with different Ge shapes. A weaker grading means a smaller value of  $\Delta V_{g,\max}$  in (3.15) leading to a smaller increase of the weight factor. For all cases, the model equation yields very accurate results. For the box profile, no grading is present, leading to  $a_{hjEi} = 0$ . In the model, a series expansion of (3.19) is used for small  $a_{hjEi}$ , which leads to  $h_{jEi} = h_{jEi0}$  for  $a_{hjEi} = 0$ . Furthermore, the singularities at  $V_{B'E'} = 0$  V and at  $V_{B'E'} = V_{DEi}$  are avoided in the model formulation.

For a Ge profile increase throughout the entire base region, i.e., including the base portion of the BC SCR, also the weight factor  $h_{jCi}$  becomes bias dependent but decreases with increasing voltage  $V_{B'C'}$ . The behavior of  $h_{jCi}$



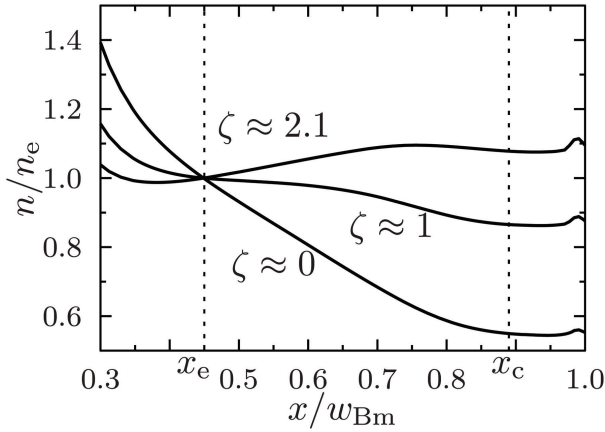
**Figure 3.5** Application of the model Equation (3.19) for the weight factor obtained from transistors with different shapes of the Ge profile [Paw15a].

can be described by a similar function as (3.19) and its own set of parameters. The value of  $h_{jCi}$  decreases with the slope of the Ge grading, which results in a reduction of the Early effect. A simple physics-based explanation for this is that the Ge grading causes a strong aiding drift field  $E_{nx}$  across the base region. Once the injected electron current density  $J_n$  is dominated by drift, the position of the BC SCR boundary  $x_c$  at the end of the neutral base has only a weak impact on the value of  $J_n$ . In other words, in a box Ge profile (i.e.,  $E_{nx} \approx 0$ )  $J_n$  is driven the diffusion gradient of the injected carriers. This is visualized in Figure 3.6 by the curve  $\zeta \approx 0$ , where

$$\zeta = -\frac{E_{nx}}{V_T/w_B} \quad (3.20)$$

represents the field factor and the normalization factor  $V_T/w_B$  corresponds to the equivalent field of a pure diffusion current. For a high field, the carrier gradient disappears as shown in Figure 3.6 for different values of  $\zeta > 0$ . Hence, moving the location of  $x_c$  does not change  $J_n$  anymore, thus resulting in the observed larger Early voltage for graded base HBTs. Since the bias dependence of the corresponding weight factor  $h_{jCi}$  is very small, no dedicated model equation for  $h_{jCi}(V_{B'E'})$  is included in HICUM/L2.

Except for the non-idealities in the transfer current at low injection that were explained before, also the increasing non-linearity of SiGe HBTs with graded Ge compared to transistors with a box Ge profile can be seen even before the onset of high-current effects. An explanation for this phenomenon

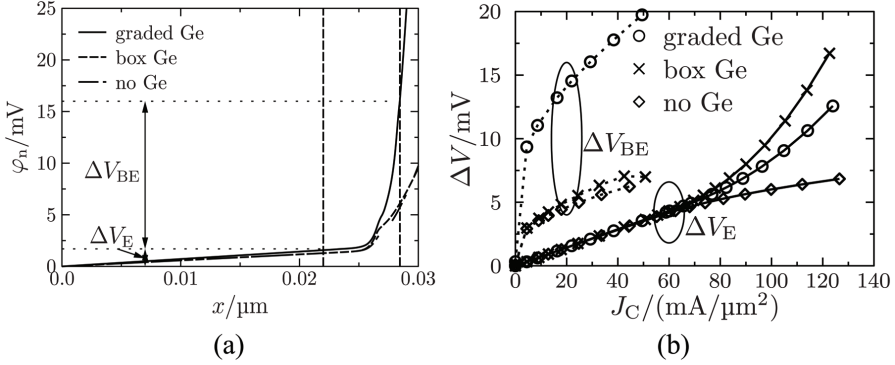


**Figure 3.6** Spatial dependence of the electron density normalized to  $n_e$  from (3.11) in the neutral base, marked by the vertical dashed lines, for different values of the field factor  $\zeta$ . The  $x$ -axis is normalized to the metallurgical base width  $w_{Bm}$  with the BE junction located at  $x = 0$ .

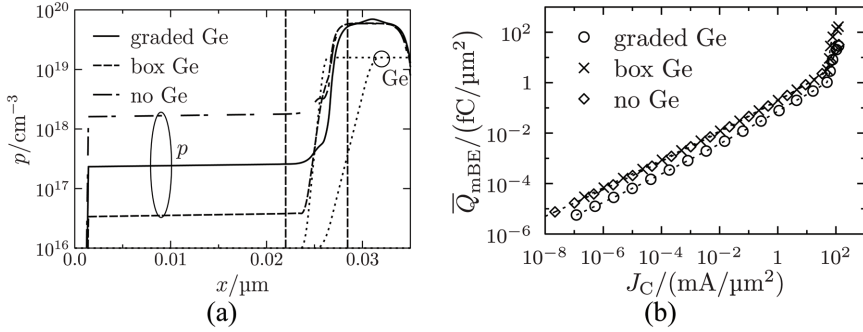
can be found by a closer look at the different parts of the mobile charges and the relation to the corresponding weight factors according to the GICCR.

The reason for the increased non-ideality is also indicated by the voltage drop from the internal emitter contact  $E'$  at  $x = 0$  to  $x = x_e$ . The voltage drop is given in Figure 3.7 for transistors with different Ge profiles. The corresponding hole densities are given in Figure 3.8(a). It can be seen that although the voltage drop in the emitter is the same for all transistors up to medium current densities, the voltage drop in the BE SCR for a given current density is significantly larger for the transistor with the graded Germanium profile. This is caused by the neutral charge in the SCR. As shown in Figure 3.8(b), for a given collector current density this charge is visibly smaller for the graded Ge compared to the box Ge. Since however the current density is defined by the electron density and the gradient of the quasi-Fermi potential, the reduced carrier density can only be compensated for by an increased voltage drop for maintaining the current density.

For modeling though, only the potential at the  $E'$  is known but the voltage drop not calculated explicitly. However, it was shown in, e.g., [Paw15a, Fri02] that a voltage drop in the internal transistor can be directly expressed by the weight function in the GICCR. The resulting weight factors for the mobile charge in the emitter,



**Figure 3.7** (a) Determination of the voltage drop in the neutral emitter ( $\Delta V_E$ ) and in the BE SCR ( $\Delta V_{BE}$ ) from the quasi-Fermi potential of the electrons for transistors with different Ge profiles in the base. The dashed lines show the begin and end of the BE SCR. (b) Current dependence of the voltage drops;  $\Delta V_{BE}$  is shown for bias points only up to the beginning of high-current effects [Paw15a].

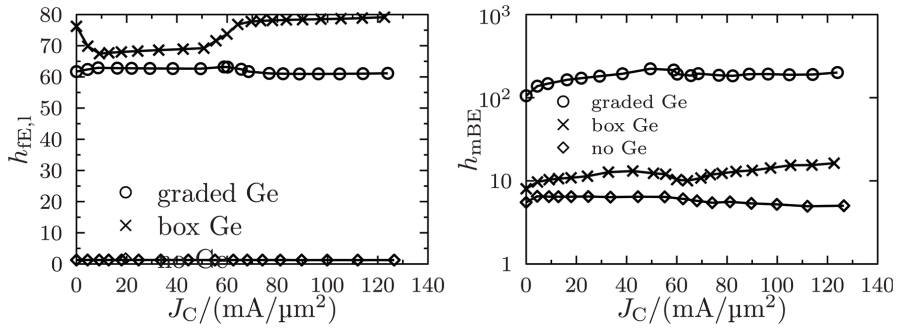


**Figure 3.8** (a) Spatial dependence of the hole density for transistors with different Ge profiles. The Ge content is given by the dotted lines for the box (left) and the graded (right) profile. The vertical dashed lines are the same as in Figure 3.7(b). (b) Minority charge as a function of collector current density in the BE SCR for transistors with different Ge profile [Paw15a].

$$h_{fE} = \frac{\overline{\mu_{nB} n_{iB}^2}}{\overline{\mu_{nE} n_{iE}^2}}, \quad (3.21)$$

and in the BE SCR,

$$h_{mBE} = \frac{\overline{\mu_{nB} n_{iB}^2}}{\overline{\mu_{nBE} n_{ijE}^2}}, \quad (3.22)$$



**Figure 3.9** Current dependence of the weight factors for the charge stored in the neutral emitter and BE SCR for the transistors with different Ge profiles [Paw15a].

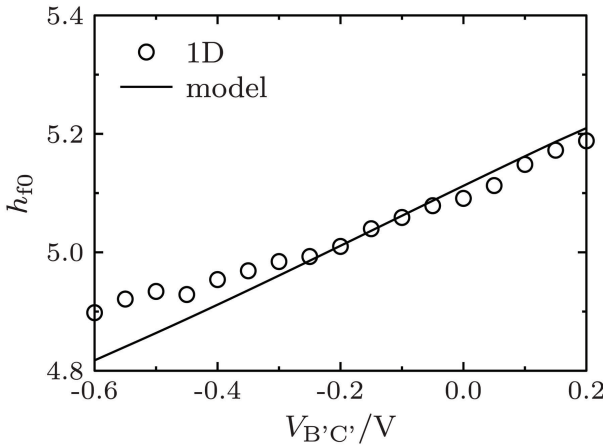
respectively, show just a weak current dependence (see Figure 3.9). While  $h_{FE,1}$  equals 1 for BJTs, it is much larger than 1 for HBTs due to the reduced band-gap in the base of the latter compared to that in the Si emitter, i.e.,  $n_{iB,\text{SiGe}} \gg n_{iB,\text{Si}}$ , but  $n_{iE,\text{SiGe}} = n_{iE,\text{Si}}$ .

The weight factor  $h_{mBE}$  is larger than 1 even for the BJT and box Ge profile due to the bandgap variation across the BE SCR caused by the doping profile (i.e., the bandgap narrowing effect). A Ge grading across the BE SCR can increase the value of  $h_{mBE}$  significantly as shown in Figure 3.9.

The low-current component of the mobile charge,  $Q_{fl} = \tau_{f0} I_{Tf}$ , is experimentally characterized by a low-current transit time  $\tau_{f0}$ , which is difficult to partition into its components from the different spatial transistor regions. Therefore, in HICUM/L2 the mobile charges in emitter, base, and BC SCR are merged into the low-current minority charge  $Q_{fl}$  [cf. (3.9)]. For describing the transfer current, a weighted charge  $h_{f0} Q_{fl}$  has to be inserted according to (3.9). For advanced SiGe HBTs, a weight factor  $h_{f0} > 1$  turned out to be necessary for modeling the transfer characteristics at medium injection levels while maintaining a physics-based value of  $Q_{p0}$ .

Two components of  $Q_{fl}$ , the one related to the neutral base and to the BC SCR exhibit a dependence on  $V_{B'C'}$ . In addition, the Ge grading also causes the weight factor of the neutral base charge to be  $V_{B'C'}$  dependent. Since the  $V_{B'C'}$  dependence is a strong function of the actual transistor design, i.e., the doping concentrations in the base and collector, only a very general model equation according to

$$h_{f0} = h_{f00}(1 + a_{hf0,c} V_{B'C'}) \quad (3.23)$$



**Figure 3.10** Bias dependence of  $h_{f0}$  extracted from 1D device simulations and application of the model equation (3.23).

is employed. The bias dependence of  $h_{f0}$  based on 1D device simulations is given in Figure 3.10. The extracted values from measured transistors are shown later in Figure 3.28.

The weight factors  $h_{fE}$  and  $h_{fC}$  for the high-current components  $\Delta Q_{fE}$  and  $Q_{fC}$  in (3.9) were already available in HICUM/L2 prior to version 2.3. For the emitter, (3.21) is applied with a bias-independent value according to Figure 3.9. The weight factor for the collector,

$$h_{fC} = \frac{\overline{\mu_{nB} n_{iB}^2}}{\mu_{nC} n_{iC}^2} \quad (3.24)$$

is only relevant at high injection since under forward operation the hole carrier density and related charge in the collector are negligible at low and medium injection.

### 3.3.3 Temperature Dependence

As outlined in the introduction of this chapter, the transfer current exhibits unique temperature effects for graded Germanium transistors compared to box transistors (or BJTs). In addition to the temperature dependence of the charge components, the weight factors play a significant role for correctly describing the temperature dependence of the transfer current. The temperature dependence of the weight factors can be derived systematically from (3.4) and is mostly related to the ratio of the intrinsic carrier densities in

the particular transistor region  $k$  via the region-specific bandgap. The general equation for the weight function temperature dependence therefore reads

$$\frac{h_k(T)}{h_k(T_0)} = \frac{\overline{\mu_{nB}(T)n_{iB}^2(T)}}{\mu_{nk}(T)n_{ik}^2(T)} \frac{\mu_{nk}(T_0)n_{ik}^2(T_0)}{\overline{\mu_{nB}(T_0)n_{iB}^2(T_0)}} \approx \frac{\overline{n_{iB}^2(T)}}{n_{iB}^2(T_0)} \frac{\overline{n_{ik}^2(T_0)}}{n_{ik}^2(T)}, \quad (3.25)$$

neglecting the temperature dependence of the mobility. Assuming a linear temperature dependence of the spatially averaged bandgap voltage  $\overline{V_{gk}}$  in a particular transistor region  $k$  yields for the corresponding ratio

$$\frac{\overline{n_{ik}^2(T)}}{n_{ik}^2(T_0)} = \left(\frac{T}{T_0}\right)^3 \exp\left[\frac{\overline{V_{gk0}}}{V_T} \left(\frac{T}{T_0} - 1\right)\right] \cong \exp\left[\frac{\overline{V_{gk0}}}{V_T} \left(\frac{T}{T_0} - 1\right)\right] \quad (3.26)$$

with  $\overline{V_{gk0}}$  as the toward  $T = 0$  extrapolated bandgap voltage. This gives for the corresponding weight factor

$$\frac{h_k(T)}{h_k(T_0)} = \exp\left(\frac{\overline{V_{gB0}} - \overline{V_{gk0}}}{V_T} \left(\frac{T}{T_0} - 1\right)\right). \quad (3.27)$$

Therefore, if the bandgap of region  $k$  is larger than that of the base region, the value of  $h_k$  will decrease with increasing temperature. Except for  $h_{jCi}$ , this is indeed the case for all weight factors in HBTs with a graded Ge profile across the entire base.

Following from (3.27), for  $h_{jEi}$  the temperature dependence of  $h_{jEi0}$  is given by the term

$$h_{jEi0}(T) = h_{jEi0}(T_0) \exp\left(\frac{\Delta V_{gBE}}{V_T} \left(\frac{T}{T_0} - 1\right)\right) \exp(a_{hjEi}(T_0) - a_{hjEi}(T)), \quad (3.28)$$

which has been changed into the more flexible model expression

$$h_{jEi0}(T) = h_{jEi0}(T_0) \exp\left(\frac{\Delta V_{gBE}}{V_T} \left[\left(\frac{T}{T_0}\right)^{\zeta_{V_{gBE}}} - 1\right]\right), \quad (3.29)$$

with

$$\Delta V_{gBE} = \overline{V_{gB0}} - \overline{V_{gjE0}} < 0 \quad (3.30)$$

and the exponent coefficient  $\zeta_{V_{gBE}}$  as model parameters. In addition to  $h_{jEi0}$ , the parameter  $a_{hjEi}$  is also temperature dependent due to  $x_{e0}(T)$  and  $V_T$  in

(3.18) and (3.15). The former can be directly expressed by the corresponding depletion capacitance  $C_{jEi0}(T)$ , the latter directly by  $T$ , yielding

$$a_{hjEi}(T) = a_{hjEi}(T_0) \frac{T_0}{T} \frac{C_{jEi0}(T_0)}{C_{jEi0}(T)} = a_{hjEi}(T_0) \frac{T}{T_0}^{\zeta_{hjEi}}, \quad (3.31)$$

where introducing the exponent coefficient  $\zeta_{hjEi}$  as model parameter provides more flexibility.

Since a large portion of  $h_{f0}$  is related to  $h_{mBE}$  which itself depends on  $V_{gE0}$  as well, a similar temperature dependence for  $h_{f0}$  is derived reading

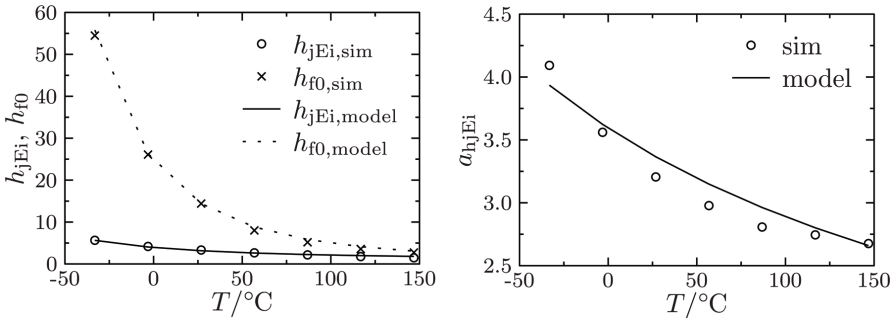
$$h_{f0}(T) = h_{f0}(T_0) \exp \left( \frac{\Delta V_{gBE}}{V_T} \left( \frac{T}{T_0} - 1 \right) \right) \quad (3.32)$$

The aforementioned model equations are compared with device simulation results in Figure 3.11, showing both the expected decrease of the weight factors and sufficiently high accuracy.

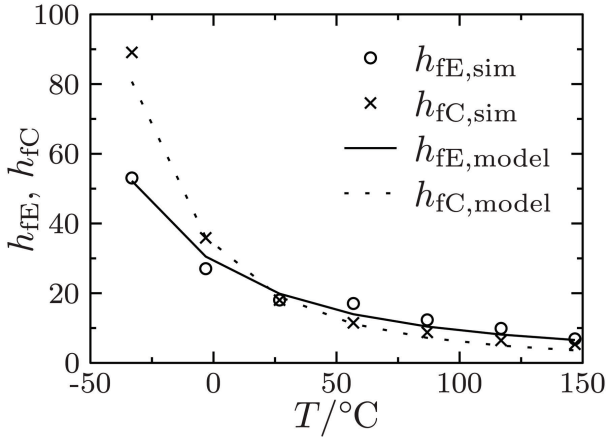
The temperature dependence of the high-current weight factors follows directly from (3.23) and (3.21).

$$h_{f(E,C)}(T) = h_{f(E,C)}(T_0) \exp \left[ \frac{\overline{V_{gB0}} - \overline{V_{g(E,C)0}}}{V_T} \left( \frac{T}{T_0} - 1 \right) \right] \quad (3.33)$$

Figure 3.12 shows the corresponding comparison with device simulation results.



**Figure 3.11** Application of the model Equations (3.29) and (3.32) to  $h_{jEi0}(T)$  and  $h_{f0}(T)$  as well as Equation (3.31) to  $a_{hjEi}$  obtained from 1D device simulations [Paw15a].



**Figure 3.12** Application of (3.33) to the high current weight factors  $h_{fE}$  and  $h_{fC}$  obtained from 1D device simulations [Paw15a].

### 3.4 Charge Storage

#### 3.4.1 Critical Current

Based on the Kirk-effect, the critical current  $I_{CK}$  characterizes the onset of high-current effects. It is modeled in HICUM/L2 by the equation

$$I_{CK} = \frac{V_{Ci}}{R_{Ci0} \left( 1 + \left( \frac{V_{Ci}}{V_{lim}} \right)^{\delta_{ck}} \right)^{\frac{1}{\delta_{ck}}}} \left[ 1 + \frac{v + \sqrt{v^2 + a_{ICKpt}}}{2} \right] \quad (3.34)$$

with  $v = (V_{Ci} - V_{lim})/V_{PT}$  as argument,

$$V_{Ci} = V_{C'E'} - V_{C'E's} \quad (3.35)$$

as effective collector voltage and  $V_{C'E's}$  as the internal CE saturation voltage, and  $V_{lim}$  corresponding to the electric field separating the ohmic from the saturation region in the velocity versus field relation.

For low values of  $V_{Ci}$  the entire epi-collector region becomes neutral at the onset of high current densities. This is represented in (3.34) by the first term, where the  $V_{Ci}$ -dependent term in the denominator models the field dependent mobility. The low-field mobility has been absorbed in the model parameter  $R_{Ci0}$ , which resembles the ohmic resistance of the entire epi-collector region with an average doping concentration  $N_{Ci}$ . The parameter

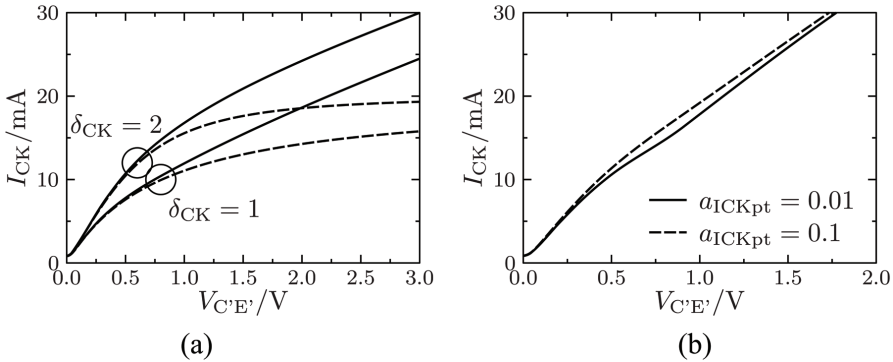
$\delta_{\text{ck}}$  was set to 2 in versions of HICUM/L2 prior to 2.3, but has recently been introduced as model parameter in order to allow a more flexible voltage-dependent (i.e., collector field) description of  $I_{\text{CK}}$  (e.g.,  $\delta_{\text{ck}} = 1$  for pnp transistors).

The last term within the square brackets in (3.34) represents the high-voltage solution which is characterized by the collector punch-through voltage

$$V_{\text{PT}} = \frac{qN_{\text{Ci}}}{2\epsilon} w_{\text{Ci}}^2. \quad (3.36)$$

While the collector doping has been continuously increasing for high-speed HBTs, the collector width  $w_{\text{Ci}}$  has decreased, yielding smaller and smaller values for  $V_{\text{PT}}$ . Furthermore,  $a_{\text{ICKpt}}$  was recently introduced as a model parameter (rather than a fixed parameter) for the hyperbolic smoothing function that connects the low- and high-voltage regions in order to provide a highly accurate modeling of the (quasi-)saturation region in the output characteristics and to avoid possible kinks due to non-physical parameter values [Cel14].

The effect of  $\delta_{\text{ck}}$  on the voltage dependence of  $I_{\text{CK}}$  is shown in Figure 3.13(a). The lower  $\delta_{\text{ck}}$  reduces the slope at lower voltages (i.e., field in the collector), but the asymptotic value for  $I_{\text{CK}}$  will be the same at very large voltages since the saturation velocity is not changed by the parameter. Figure 3.13(b) exhibits the impact of  $a_{\text{ICKpt}}$ . The possible kink in  $I_{\text{CK}}$  for too small values of  $a_{\text{ICKpt}}$  can be clearly observed.



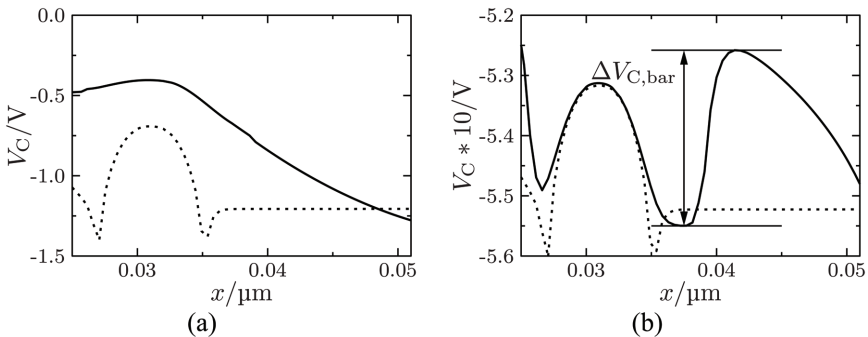
**Figure 3.13** (a) Impact of  $\delta_{\text{ck}}$  on the voltage dependence of  $I_{\text{CK}}$ . Solid lines show the actual  $I_{\text{CK}}$  while dashed lines show the results for the low-voltage portion of [i.e., the first term of (3.34), neglecting punch-through]. (b) Impact of  $a_{\text{ICKpt}}$  on  $I_{\text{CK}}$  for a very small punch-through voltage.

### 3.4.2 SiGe Heterojunction Barrier

The changing composition from SiGe back to Si within the BC SCR causes a barrier in the valence band. Due to the very small difference in electron affinity between Si and SiGe (for typical Ge concentrations not exceeding 30%), this barrier is almost completely given by the difference in bandgap between the Ge (peak) location and the pure Si collector region. For low current densities and CE voltages beyond strong saturation, the barrier is typically masked by the electric field in the BC SCR. However, at high current densities the electric field in the BC SCR starts collapsing due to the compensation of  $N_{Ci}$  by a high mobile carrier concentration. Since the BC barrier initially prevents holes from being injected into the collector (unlike in a BJT) not only the increase in electron current density with  $V_{B'E'}$  becomes limited but also a dipole layer starts to form around the barrier [Sch10]. This leads to a shift of the barrier height from the valence band into the conduction band and hole injection from the base into the collector to enable a further increase in current density via additional diffusion. The formation of the barrier is highlighted in Figure 3.14 where also the barrier height in the conduction band,  $\Delta V_{C,bar}$ , is defined for the case of high current densities.

Resulting from observing its current dependence, the barrier height in HICUM/L2 is modeled by a simple empirical expression,

$$\Delta V_{C,bar} = V_{C,bar} \exp \left( - \frac{2}{i_{bar} + \sqrt{i_{bar}^2 + a_{Cbar}}} \right), \quad (3.37)$$



**Figure 3.14** Spatial dependence of the conductance band edge for low and high current densities (solid lines), highlighting the presence of the barrier at high current densities. The dashed line shows the doping profile of the transistor just for reference.

with the normalized current

$$i_{\text{bar}} = \frac{I_{\text{Tf}} - I_{\text{CK}}}{I_{\text{C,bar}}} \quad (3.38)$$

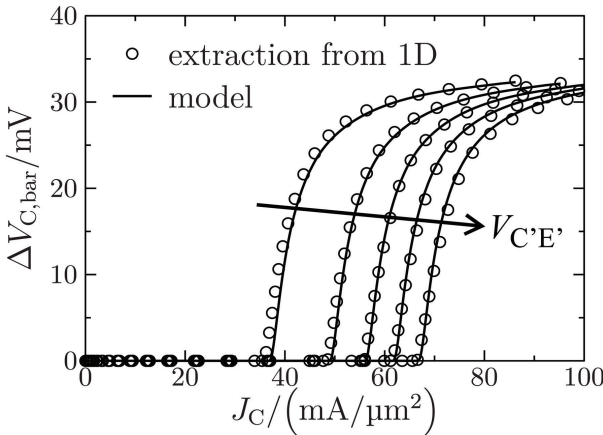
The model is based on the observation that, independent of the collector voltage, the barrier shows almost the same current dependence starting from an onset current. For the latter,  $I_{\text{CK}}$  is used since usually this onset current correlates with the classical Kirk-effect as long as the barrier is located not too far away from the metallurgic junction in the collector. Figure 3.15 shows the current dependence of  $\Delta V_{\text{C,bar}}$  obtained from 1D device simulation in comparison with (3.37) for a wide range of (internal) CE voltages.

The impact of the BC barrier on the mobile charge and associated transit time is split into two distinct components [Sch10]. First, the charge storage contribution in the base region caused by the BC barrier only is calculated by

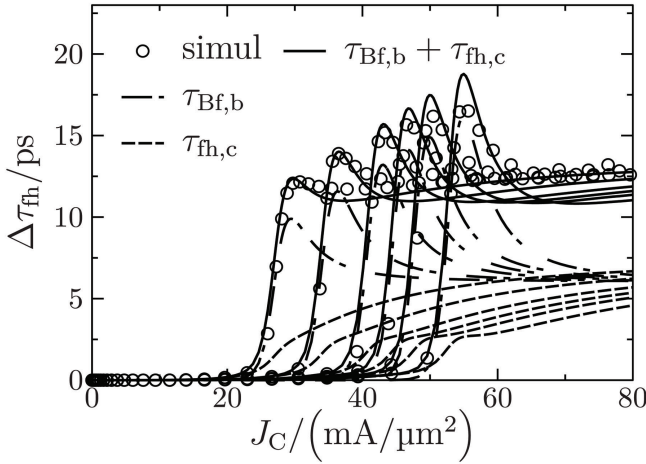
$$\Delta Q_{\text{Bf,b}} = \tau_{\text{Bfvs}} I_{\text{Tf}} \left[ \exp \left( \frac{\Delta V_{\text{C,bar}}}{V_{\text{T}}} \right) - 1 \right]. \quad (3.39)$$

Second, the classical high-injection charge in the collector and its associated base component (triggered by the collector related high-current effect) [Sch99] is extended by a barrier term,

$$\Delta Q_{\text{fh,c}} = \tau_{\text{hCs}} I_{\text{Tf}} w^2 \exp \left( \frac{\Delta V_{\text{C,bar}} - V_{\text{C,bar}}}{V_{\text{T}}} \right), \quad (3.40)$$



**Figure 3.15** Modeling of the current dependence of the heterojunction barrier voltage for different voltages  $V_{\text{C'E'}/V} = [0.3; 0.6; 0.9; 1.2; 1.5]$ .



**Figure 3.16** Transit times of a SiGe HBT showing the BC barrier effect: comparison of Equations (3.39) and (3.40) with results from 1D device simulation for different voltages  $V_{C'E'}/V = [0.3; 0.5; 0.8; 1.0; 1.2; 1.5]$ .

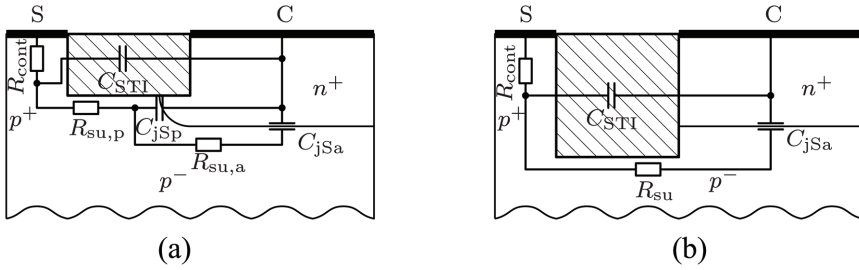
which causes a delayed nonlinear increase until the barrier is built up in the conduction band. Figure 3.16 shows the corresponding transit times obtained from the charge formulations above as

$$\tau = \left. \frac{dQ}{dI_{Tf}} \right|_{V_{C'E'}} \quad (3.41)$$

and compared to 1D device simulation results. The different components according to (3.39) and (3.40) are drawn separately as well as their sum which yields the small-signal transit time seen at the terminal of the 1D transistor.

### 3.5 Intra-Device Substrate Coupling

At high frequencies, the signal coupling between the collector of a transistor and its surrounding substrate can strongly affect the small-signal behavior, especially the HF output impedance. Different signal paths have to be distinguished. Since the collector (i.e., the buried layer) of a Si-based HBT usually forms a pn junction with the substrate, a signal path to the bulk substrate contacts exists across the area component of the CS junction capacitance  $C_{jSa}$  in Figure 3.17. In addition, a signal path through the perimeter junction and shallow or deep trench exists which is represented by  $C_{jSp}$ ,  $C_{STI}$ , and  $C_{DTI}$

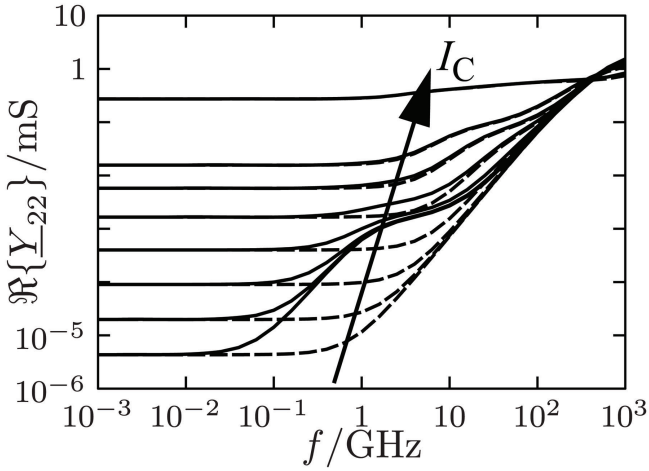


**Figure 3.17** Sketch of the cross section for (a) a junction isolated (with partial trench-isolation) and (b) a deep trench isolated collector including all relevant elements of the most simple equivalent circuit for modeling intra-device substrate coupling. Note that for all series resistance a parallel capacitance exists due to the permittivity of the substrate and that due to changes of the substrate-collector SCR all depletion capacitances  $C_{jS(a,p)}$  and series resistances  $R_{su,(a,p)}$  are bias dependent [Sch10, Paw15a].

in Figure 3.17. This perimeter path is much shorter than the bulk path if the substrate contact surrounds the transistor and is placed as close as possible to the collector, which is the case for device characterization in test structures. This coupling effect is called *intra-device* coupling. However, in circuits the situation is quite different since typically the surrounding substrate contact is omitted and the substrate is contacted somewhere on the chip. In this case, not only the transistor output impedance has a different frequency dependence but there is also signal coupling though the substrate directly between transistors. This effect is called *inter-device* substrate coupling. Both intra- and inter-device coupling are strongly layout dependent.

It is important to understand for both modelers and circuit designers that the CMs delivered in PDKs should be consistent with the p-cells offered to circuit designers. If the p-cells do not contain a surrounding substrate contact (in contrast to the characterization structures), then the PDK model should not include intra-device coupling. In this case, in which the circuit layout is unknown to the modeling engineers, it is the responsibility of the circuit designer to determine the substrate coupling and cross-talk related impedance network for each (critical) transistor!

In this section, the discussion is limited to intra-device coupling with a connected substrate ring. The general impact of the signal coupling on the output conductance  $g_o = \text{Re}\{Y_{22}\}$  is visualized in Figure 3.18. It can be seen that, for low and medium current densities, substrate coupling leads to a strong increase of  $g_o$  already at lower frequencies. This increase is proportional to the square of the frequency.



**Figure 3.18** Impact of intra-device substrate coupling on the dynamic output-conductance given by the real part of  $Y_{22}$ . Solid lines show the actual values including substrate coupling while the dashed lines show results with an ideally open substrate.

The elements of the equivalent circuit in Figure 3.17 follow directly from the transistor structure. The direct path between the collector and the substrate may be represented either by the CS perimeter depletion capacitance  $C_{jSp}$  for the case of pure junction isolation or by a bias-independent (at least to first order) deep trench oxide capacitance  $C_{DTI}$  in case of a deep trench isolation. For a combination of a shallow trench and junction isolation, a combination of bias-dependent and -independent capacitances is required. Depending on the spatial distance between the junction and the substrate contact significant series resistances can exist in the various signal paths. For each of the bulk related series resistances a parallel capacitance  $C_{Su}$  exists due to the permittivity of the substrate.

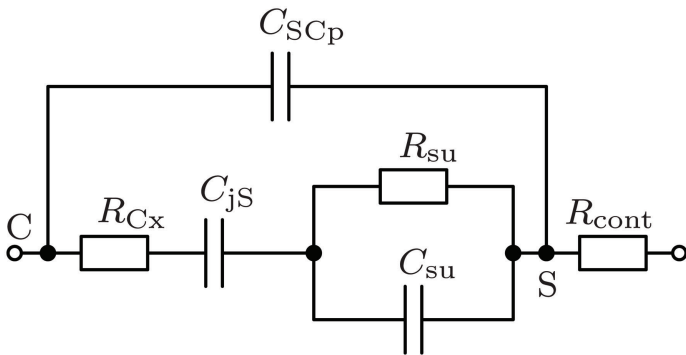
All elements given in Figure 3.17 are lumped elements which represent highly distributed effects that depend on the transistor dimensions and the operating frequency. Therefore, even more complicated equivalent circuits than the one in Figure 3.17 may be required to correctly capture the frequency behavior of the output impedance at mm- and sub-mm-wave frequencies. For accurately capturing the impact of intra- and inter-device coupling, the topology of the respective equivalent circuit along with its element values can generally only be obtained from analyzing the actual layout of all components *after* designing the circuit.

In HICUM/L2 the equivalent circuit shown in Figure 3.19 was chosen which is capable of capturing intra-device substrate coupling as it is encountered during device characterization and model parameter extraction as well as during circuit design if p-cells with surrounding substrate contacts are employed. In Figure 3.19, C and S are the terminal collector and substrate contact,  $R_{Cx}$  is the external collector resistance,  $C_{jS}$  is the bottom component of the SC depletion capacitance, and  $R_{Su}$  and  $C_{Su}$  represent the connection through the bottom part of substrate. These elements correspond to  $C_{jSa}$  and  $R_{Su}$  (in Figure 3.17(b)) or  $R_{Su,a}$  (in Figure 3.17(a)), respectively.

The perimeter substrate capacitance  $C_{SCp}$  follows from  $C_{STI}$  and  $C_{jSp}$  where it is important to realize that in case of a combined trench and junction isolation (cf. Figure 3.17(a)) portions of  $C_{jSp}$  may be included in  $C_{jS}$  depending on the width of the trench oxide and therefore the value of  $R_{Su,p}$ .

The additional series resistance  $R_{cont}$  along the side-wall of the trench-oxide is not included in the CM in order to reduce the node count for low-frequency operation. As demonstrated in Figure 3.19 it can be connected to the substrate terminal of the CM in a subcircuit. Similar to the discussion for  $C_{SCp}$ , the spatial dimensions and relations between the circuit element values define whether  $R_{Su,p}$  (if present) is merged into  $R_{cont}$  or  $R_{Su}$ .

In contrast to  $C_{jS}$  which is modeled depending on the internal SC voltage  $V_{S'C'}$ , the bias dependence of  $C_{SCp}$  can be activated or deactivated by the user to include the contributions of the perimeter depletion capacitance and the constant trench oxide, respectively.



**Figure 3.19** Substrate coupling equivalent circuit in HICUM/L2.

### 3.6 SiGe HBT Parameter Extraction

For various reasons, it should *not* be attempted to determine the parameters of a sophisticated physics-based compact HBT model such as HICUM/L2 from the characteristics of just a single transistor<sup>3</sup>. First, the equivalent circuit represents still to some extent the distributed device structure; for instance, there are internal and perimeter related elements. Also, the transfer current results from a well-defined transformation of a two-transistor behavior into a single transistor representation (cf. the effective emitter area section later) and, e.g., the series resistance values are scaled based on sheet or contact resistivities and device dimensions. The information corresponding to those partitionings and transformations can simply not be obtained from measurements on a single device. Second, a one-hat-fits-all single-device geometry is never being used in analog RF circuit design. In fact, exploiting a process technology (and amortizing the cost for its development as rapidly as possible) requires optimizing the circuits by using suitable and typically different transistor sizes and configuration for the different applications even within the circuits. This requires to cover a certain range of device sizes during parameter extraction. Third, utilizing device size adds another independent dimension and set of data points for determining the unknown parameters and increases the chances for obtaining physics-based parameter values. The number of independent data can be increased by adding special test structures to the (test) transistors. Fourth, only a physics-based set of parameters maximizes the use of a physics-based CM by enabling statistical and predictive circuit design and modeling.

An extraction follows a certain procedure that is preferably designed such that as many as possible model parameters are determined independently. The description below will reflect that sequence, starting with an overview of series resistance determination. Then, the methods for those parameters are covered that have been introduced in the extended equations. Finally, an extended concept for geometry-scalable parameter extraction is described.

Compact models are supposed to represent the typical characteristics of a process. For their first delivery along with the process qualification only limited statistics are available which need to be utilized though for selecting a proper die for parameter extraction. Since it is unlikely that all process control monitor values of an available die match all their nominal values from

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<sup>3</sup>Reasonable results have been obtained though for at least all parameters related to the internal transistor after careful deembedding of all external elements and heavy utilization of optimization [Ros13].

wafer tests, the extracted model parameters need to be “shifted” properly (e.g., [Sch05]) to the nominal values. This is possible only with a physics-based model or, more precisely, with the associated model parameters having a clear physics-based relation to process parameters.

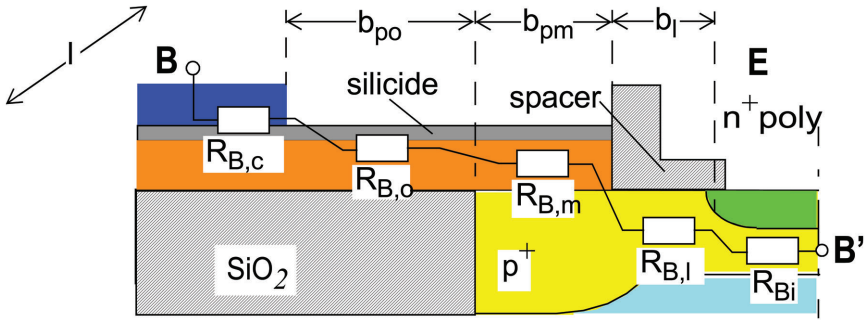
### 3.6.1 Extraction of Series Resistances

Preferably, a series resistance can be determined from its components as shown in Figure 3.20 for the example of the base region. Each different structural region in the cross section is represented by a resistor element. The value of the latter can always be calculated from a specific resistivity, the length of the region in direction of the current flow ( $b$ ), and its cross-sectional area. Except for contacts, semiconductor layers are typically characterized by the sheet resistance  $r_S$ , which eliminates the need for knowing the spatially dependent vertical doping profile and reduces the cross-sectional area to the lateral layout dimension ( $l$ ) perpendicular to the current flow. Contact resistances are calculated either from an area-specific resistivity (in  $\Omega\mu\text{m}^2$ ) if the current crosses the contact cross-sectional area vertically or from a length-specific resistivity (in  $\Omega\mu\text{m}$ ) if the current flows to the side. The contact in Figure 3.20. belongs to the latter category. Thus, the overall external base series resistance of the structure example in Figure 3.20 reads:

$$R_{Bx} = \underbrace{\frac{\rho_{B,c}}{l_{Bc}}}_{\text{Contact}} + \underbrace{r_{BS,po} \frac{b_{po}}{l_{B,po}}}_{\text{poly-Si on oxide}} + \underbrace{r_{BS,pm} \frac{b_{pm}}{l_{B,pm}}}_{\text{mono-Si on poly-Si}} + \underbrace{r_{BS,l} \frac{b_l}{l_{E,l}}}_{\text{Link (spacer)}} \quad (3.42)$$

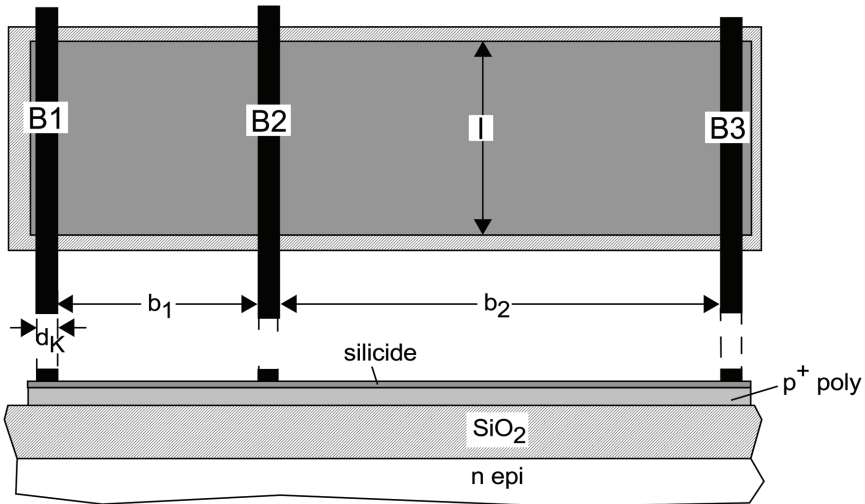
where  $\rho_{B,c}$  is the base contact resistivity,  $r_{BS,ab}$  is the sheet resistance of the region “ab,” and the  $b_{ab}$  and  $l_{ab}$ , respectively, are the widths and (effective) lengths of each region.

The form (3.42) allows to calculate the base series resistance for all sizes and even for changes in the dimensions and doping profiles as they occur during fabrication (resulting in process tolerances) and process development. A general and accurate formulation of (3.42) can be found in [Sch08a, Sch10], which is applicable to all common contact configurations and SiGe HBT architectures. Obviously, to employ (3.42) for generating  $R_{Bx}$  for a given HBT device size, the parameters of each component need to be known. The determination of the actual (i.e., not drawn) dimensions can be obtained from TEM and SEM measurements. Once the process is qualified, the relation between each actual and drawn dimension can be established, so that for



**Figure 3.20** Illustration of the base series resistance components and their relation to the HBT cross section (schematic).

model generation the (drawn) layout dimension can be used. The specific contact and sheet resistance can be determined based on very simple (DC) test structures [Sch88, Sch08b] as shown in Figure 3.21 for the example of the contact and poly-on-mono region. Forcing a current from B1 and B3 and measuring the voltage drops between (a) B1 and B3 and (b) B1 and B2 using a Kelvin contact configuration gives two resistance values for the two unknowns  $\rho_{B,c}$  and  $R_{BS,po}$ . Extending the structure to include more base



**Figure 3.21** Typical test structure (a.k.a. contact chain) used for determining the specific electrical resistivities of the external base resistance components. B1, B2, B3 designates the contacts.

layers (as in Figure 3.20) allows the successive determination of all other sheet resistances. The principle described above can be applied also to the determination of the components of the external collector resistance.

From transistor theory (e.g., [Pri67, Sch10]), the bias-dependent internal DC base resistance is generally given by

$$R_{Bi} = r_{SBi} \frac{w_E}{l_E} g_i(b_E, l_E) \Psi_{dc}(I_{Bi}, r_{SBi}, b_E, l_E), \quad (3.43)$$

where  $r_{SBi}$  is the sheet resistance of the internal base region (i.e., under the emitter),  $b_E(l_E)$  is the (effective) emitter width (length),  $I_{Bi}$  is the internal base current,  $g_i$  is a geometry factor that takes into account all common emitter shapes [Sch91, Sch92, Sch10], and  $\Psi_{dc}$  is the emitter current crowding function. The latter can be neglected (i.e.,  $\Psi_{dc} = 1$ ) for all modern SiGe HBT process technologies. For a given HBT size, only the zero-bias sheet resistance

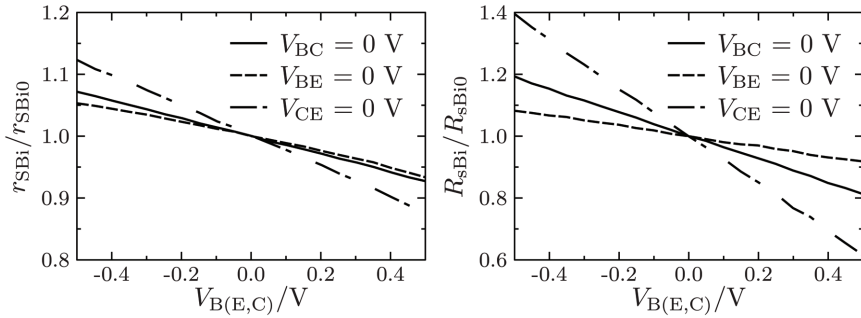
$$R_{Bi0} = r_{SBi0} \frac{w_E}{l_E} g_i(w_E, l_E), \quad (3.44)$$

is required as parameter in HICUM. Hence,  $r_{SBi0}$  needs to be extracted from measured data. The test structure of choice here is the transistor tetrode [Sch88, Rei91, Sch07]. The principle method for extracting  $r_{SBi}$  over a wide reverse and forward bias range *under simultaneous transistor operation* is described in detail in [Rei91]. There have been other proposals on how to utilize the tetrode for determining  $r_{SBi}$  or  $R_B$ . Most recently [Sch17], the existing methods have been applied to various advanced process technologies. The corresponding comparison clearly indicates that the method in [Rei91] is the most accurate over the widest bias range (including even high the high-current region).

Furthermore, the extracted bias-dependent sheet resistance of the internal base,  $r_{SBi}$ , is utilized to determine the zero-bias hole charge of the transistor  $Q_{p0}$ , which is required for the accurate calculation of the transfer current. Due to the Early-effect and injected minority charge, the base sheet resistance

$$r_{SBi} \cong r_{SBi0} \frac{Q_{p0}}{Q_{p0} + Q_{jEi} + Q_{jCi} + Q_f}, \quad (3.45)$$

is modulated by the voltages of both SCRs through the depletion charges  $Q_{jEi}$  and  $Q_{jCi}$  and the diffusion charge  $Q_f$ . Note that above equation is slightly simplified by neglecting the bias dependence of the hole mobility. Figure 3.22. shows the extracted  $r_{SBi}$  curves in the low bias range for two different technologies. In each case, the different bias conditions lead to a



**Figure 3.22** Internal base sheet resistance, normalized to its zero-bias value  $r_{sBi0}$ , as extracted from tetrodes for different bias conditions and technologies.

different contribution of the depletion charges in (3.45), while mobile charge is negligible in all cases. The stronger impact of the BE junction charge compared to the BC junction charge is clearly visible by the larger slope for  $V_{BC} = 0$  V. Also, for the technology on the r.h.s. a larger impact of the space charges on  $Q_{p0}$ , can be observed, indicating a lower base doping at a similar width.

While it is possible for BJTs (i.e., bipolar technologies until the early 1990s) to determine the emitter resistance from dedicated test structures, this has become impossible for modern SiGe HBTs. The reason for this is that the by far largest contribution to the emitter resistance still comes from the interface between the poly- and mono-silicon, but that its formation is intrinsically coupled to the emitter (poly-)layer formation; i.e., there is no separate emitter implant anymore. Therefore, the emitter resistance has to be measured directly on a HBT structure (see below). But this should be done on various geometries in order to obtain the simple and usually sufficient scaling equation,

$$R_E = \rho_{E,C}/A_{E0} \quad (3.46)$$

for a single emitter window. Here,  $\rho_{E,c}$  is the poly-to-mono-Si contact resistivity and  $A_{E0}$  is area of this interface, which corresponds to the area of the actual emitter window opening.

Some modelers still question the accuracy of transistor theory and prefer to determine series resistances directly from a given HBT structure. Over the past >60 years of bipolar transistor technology development, many different methods were proposed. There often quite different results can become confusing especially for young modeling engineers and the question arises which of these methods work at all and which ones are actually applicable

to advanced SiGe HBT technologies. To answer these questions, recently several studies on the extraction methods for base, collector and emitter resistance have been completed, in which the various methods were applied to SiGe HBTs with widely varying emitter sizes from six different process technologies, ranging from established production to the most advanced prototyping processes. In all cases, the (absolute) accuracy of each method was assessed by applying it to a complete HICUM/L2 model for the particular process and comparing the obtained resistance with the known one of the model. This approach also allows the investigation and identification of the causes of observed failures. The results are briefly summarized below; for detailed results, the reader is referred to the corresponding references.

In [Kra15], a comprehensive and detailed study of nine widely used methods (and their variants) for extracting the emitter resistance  $R_E$  is presented. Using high-performance and high-voltage devices with a wide range of up to 12 emitter sizes, the results of this study are believed to be representative for the actual accuracy and applicability of the various  $R_E$  extraction methods. It was found that *none* of the existing methods works reliably across *all* process technologies. The most important causes of deviations are the strongly simplified equivalent circuit and the neglect of important physical effects (such as high-injection, CB barrier effect, self-heating) in the derivation of the methods. The two methods working mostly are the ones in [Paw14b, Hue04], but the one in [Paw14b] is based on the occurrence of self-heating. Methods based on fly-back/open-collector and impact-ionization, which increase the risk of device destruction, are not reliable in practice. This also applies to HF small-signal methods, where the impact of  $R_E$  is masked by the much higher base resistance. The Ning-Tang method is the least reliable of all methods.

A detailed quantitative analysis of the most widely used methods for determining the base resistance directly from a transistor was performed in [Paw16] for a wide range of emitter geometries. The CM-based assessment clearly revealed that all methods only enable the extraction of the external base resistance, while the determination of the internal (bias dependent) base resistance is either impossible or, at best, limited to just a very narrow bias range, typically at very high injection, and are not very accurate. Small-signal HF methods, when operated at very low  $V_{CE}$  values, yield the best results, although still not with reliable accuracy across all technologies. A major cause of the failure or inaccuracy of the DC-based methods is self-heating. Thus, the use of DC operation-based methods cannot be recommended since self-heating will rather increase in future technologies. The application of the extraction methods to experimental data confirmed the large spread in the

$R_{Bx}$  results (for the same transistor structure) that was already observed from the CM. From both experimental and model based data, it was found that although some methods work reasonably well for some process technologies no method yields reliable accuracy for *all* technologies. Overall, it can be concluded that an accurate determination of both the *total* base resistance  $R_B$  and the external base resistance  $R_{Bx}$  from widely used single-transistor-based methods is highly unreliable even if small-signal methods are employed.

Finally, a comprehensive and detailed study of eight widely used methods (and their variants) for extracting the DC collector series resistance was presented in [Paw18]. Again, no method yielded accurate and reliable results across all technologies. But RF methods that rely on just a simple equivalent circuit, some of the substrate transistor-based methods, and the open-emitter method, yield overall the best results. The most important causes of deviations are the neglect or too strong simplification of the description of important physical effects (such as self-heating, high-injection). Note, the none of the methods yields any reasonable result for the bias-dependent internal collector resistance.

The recommendation for all single HBT-based series resistance extraction methods is to apply them to the utilized CM again in order to verify whether the same result is obtained. If not, then the method is unsuitable for the chosen model (equivalent circuit).

### 3.6.2 Extraction of the Transfer Current Parameters

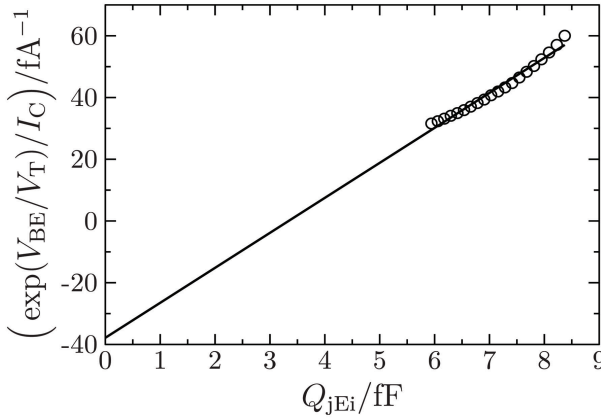
The extraction of the parameters for the transfer current of HICUM/L2 can be applied based on the methods described in [Ber02, Paw11]. The usual method is to consider different operating ranges, where only a single or very few unknown parameters exist. The most convenient way is to start with the low current weight factors  $h_{jEi}$  and  $h_{jCi}$  for the depletion charges. The extraction of the latter is not discussed here further.

For  $V_{BC} = 0$  V and low  $V_{BE}$ , where the voltage drop across the series resistances is negligible, the DC collector current is expressed by

$$I_C = I_T = \frac{c_{10}}{Q_{p0} + h_{jEi}Q_{jEi}} \exp\left(\frac{V_{BE}}{V_T}\right). \quad (3.47)$$

The method described in [Ber02] rewrites the above equation as

$$\frac{\exp(V_{BE}/V_T)}{I_T} = \frac{Q_{p0}}{c_{10}} + \frac{h_{jEi}}{c_{10}}Q_{jEi} = f(Q_{jEi}). \quad (3.48)$$



**Figure 3.23** Extraction of  $h_{jEi}$  based on (3.48).

Using the physics-based value for  $Q_{p0}$  extracted from tetrodes, the parameters  $c_{10}$  and  $h_{jEi}$  can be extracted from the slope and intercept of the above function  $f(Q_{jEi})$ . Results for applying this method to transistors with a graded Ge profile in the base are visualized in Figure 3.23. As can be seen, the data obtained from measurements do not yield a straight line as expected from (3.48) but show a curvature. Depending on this curvature, the extraction may yield a non-physical negative value for the intercept with the y-axis, given by  $Q_{p0}/c_{10}$ . The curvature is caused by the non-constant  $h_{jEi}$  present for transistors with a graded Ge profile. Hence, according to (3.19), the parameter  $a_{hjEi}$  enters into (3.48) as an additional unknown. While the method in [Paw11] works reliably for numerical device simulations due to the optimal accuracy of the results (i.e., no impact of measurement noise), results may become unreliable due to small noise in the measurements. The method in [Ste12] is based on a known saturation current and a normalized  $h_{jEi}$ , which are not so simple to extract without known  $a_{hjEi}$ .

In this section, an alternative method is presented which is based on [Ste12] without involving the additional unknown. Rather than performing a linear fit, taking the derivative of (3.48) leads to the differential equation

$$C = f(V_{BE}) + \frac{df(V_{BE})}{dV_{BE}} \frac{Q_{jEi}}{C_{jEi}} \quad (3.49)$$

with

$$f(V_{BE}) = \frac{h_{jEi}(V_{BE})}{c_{10}} \quad \text{and} \quad C = \frac{d \left[ \frac{\exp(V_{BE}/V_T)}{I_T} \right]}{dQ_{jEi}}. \quad (3.50)$$

This differential equation can be solved numerically, requiring an initial value  $f_1 = f(V_{BE1})$  with  $V_{BE1}$  being the minimum  $V_{BE}$  with reliable current values. For calculating  $a_{hjEi}$ , (3.19) is altered into

$$\begin{aligned} f &= f_1 \frac{\exp\left(a_{hjEi} \left( \left(1 - \frac{V_{BE1}}{V_{DEi}}\right)^{z_{Ei}} - \left(1 - \frac{V_{B'E'}}{V_{DEi}}\right)^{z_{Ei}} \right) - 1}{a_{hjEi} \left( \left(1 - \frac{V_{BE1}}{V_{DEi}}\right)^{z_{Ei}} - \left(1 - \frac{V_{B'E'}}{V_{DEi}}\right)^{z_{Ei}} \right)} - 1 \\ &= f_1 \frac{\exp(u) - 1}{u}, \end{aligned} \quad (3.51)$$

i.e., shifting the reference from  $V_{B'E'} = 0$ , as it is the case in (3.19), to  $V_{B'E'} = V_{BE1}$ . Note that  $c_{10}$  is a constant value and, therefore, does not change the shape of the resulting curve. Defining  $w = f/f_1$  according to [Stel2] allows the calculation of  $u$  by

$$u = -\frac{1}{w} - W_{-1} \left\{ -\frac{1}{w} \exp\left(-\frac{1}{w}\right) \right\}, \quad (3.52)$$

with  $W_{-1}$  being the negative branch on the Lambert-W function, and finally  $a_{hjEi}$  by

$$a_{hjEi} = \frac{u}{\left(1 - \frac{V_{BE1}}{V_{DEi}}\right)^{z_{Ei}} - \left(1 - \frac{V_{B'E'}}{V_{DEi}}\right)^{z_{Ei}}}, \quad (3.53)$$

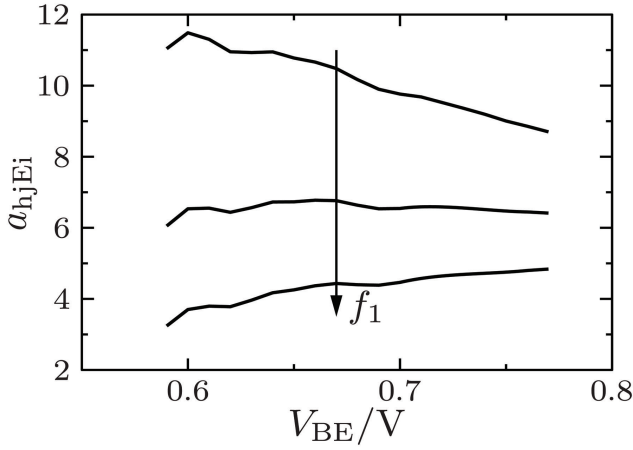
The form of the extracted curve for  $f$  from (3.49) strongly depends on the chosen initial value  $f_1$ . Therefore, if the shape does not agree with that of the model equation, a non-constant  $a_{hjEi}$  is extracted.

The actual extraction therefore is based on an iterative change of  $f_1$  until the relative standard deviation of  $a_{hjEi}$  is minimized, i.e., the most constant  $a_{hjEi}$  is obtained. A bi-section method is a reliable choice for the algorithm here. The application is visualized in Figure 3.24. Usually, for too small values of  $f_1$ , a decreasing curve of  $a_{hjEi}$  is obtained while too large values of  $f_1$  lead to increasing values. The center curve in the plot shows the actual solution of the iteration.

The remaining steps for extracting  $h_{jEi0}$  and  $c_{10}$  follow [Paw11]. Utilizing the extracted  $a_{hjEi}$ , (3.48) is altered to

$$\frac{\exp(V_{BE}/V_T)}{I_T} = f(hQ_{jEi}) \quad (3.54)$$

with  $h = h_{jEi}/h_{jEi0}$  from (3.19), where  $a_{hjEi}$  is the only parameter entering, which resolves the bending of the extraction curve and leads to the correct signs of the extracted parameters as demonstrated in Figure 3.25.

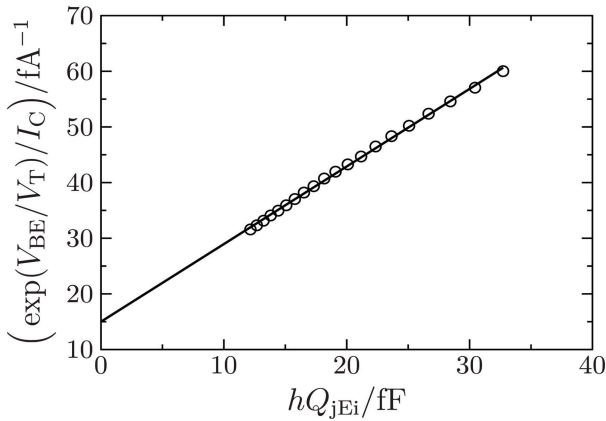


**Figure 3.24** Extraction results for  $a_{hjEi}$  based on (3.53) for different starting values  $f_1$ .

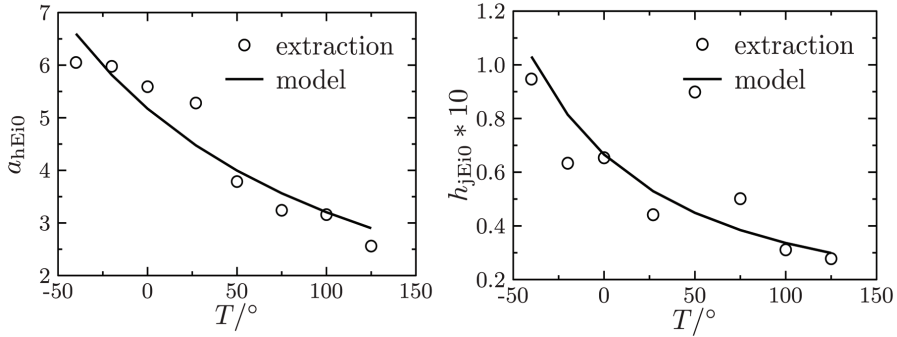
A linear extrapolation finally allows extracting  $c_{10}$  and  $h_{jEi0}$  from

$$c_{10} = \frac{Q_{p0}}{y_0} \text{ and } h_{jEi0} = \frac{m}{y_0} Q_{p0} \quad (3.55)$$

with  $m$  being the slope of the straight line and  $y_0$  the intercept with the y-axis. The extraction is performed at low injection, where series resistances and self-heating have only negligible impact during extraction of  $h_{jEi}$



**Figure 3.25** Extraction of  $h_{jEi}$  based on (3.54) including the correction based on the extracted  $a_{hjEi}$ .



**Figure 3.26** Extraction results and application of the temperature model for  $a_{h_{jEi}}$  (3.31) and  $h_{jEi0}$  (3.29).

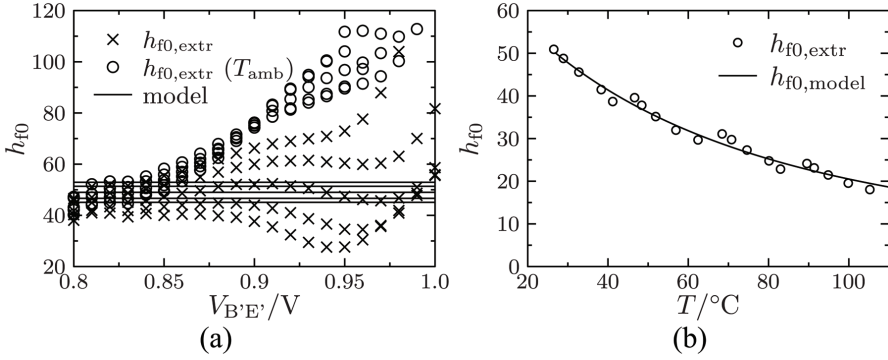
and  $c_{10}$ . Therefore, the values for  $a_{h_{jEi}}$ ,  $h_{jEi0}$ , and  $c_{10}$  are extracted for the given ambient temperature. Results are shown in Figure 3.26.

The extraction of the high-current weight factors is performed by step-wise inclusion of the related diffusion charges from (3.9). For obtaining correct results, the voltage drops across the series resistances as well as the actual device temperature due to self-heating have to be calculated. Starting with the low-current minority charge  $\tau_{f0}I_{Tf}$ , the weight factor is calculated from

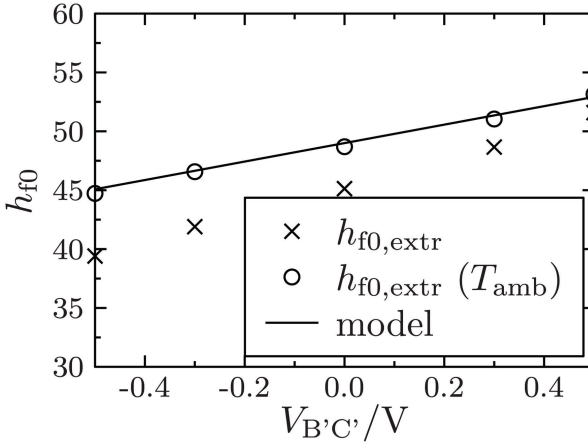
$$h_{f0} = \frac{c_{10}}{I_T} \exp\left(\frac{V_{B'E'}}{V_T}\right) - (Q_{p0} + h_{jEi}Q_{jEi} + h_{jCi}Q_{jCi}). \quad (3.56)$$

The application of above equation to data in Figure 3.27 shows a bias dependence of  $h_{f0}$ , which has to be obtained at low current densities though, yielding the results shown in Figure 3.27(b). The increase at high current densities in Figure 3.27(a) is caused by the so-far-neglected charge components and does not yield the correct  $h_{f0}$ .

The temperature dependence of  $h_{f0}$  in Figure 3.27(b) exhibits visible steps between the values of different temperature ranges. They are caused by the  $V_{BC}$  dependence of  $h_{f0}$ . Extracting  $h_{f0}$  for a given ambient temperature yields the results displayed as crosses in Figure 3.28. Since these values are still affected by the self-heating-related temperature increase inside of the device, applying the temperature dependence given in Figure 3.27(b) and correcting only the changes due to self-heating effects yields the results given by circles in Figure 3.28 which still displays a weak bias dependence.



**Figure 3.27** Extracted values for  $h_{f0}$  from (3.56) for (a) room temperature and different  $V_{BC}$ . (b) Extracted values chosen at low current densities for different temperatures and  $V_{BC}$  [Paw15a].

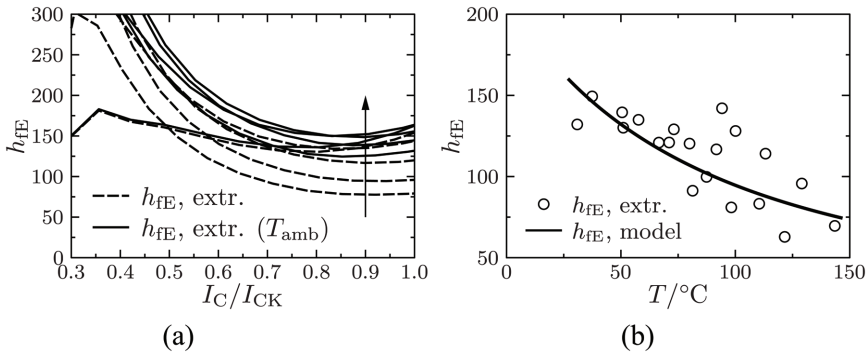


**Figure 3.28** Extraction results for the bias-dependent  $h_{f0}$  at room temperature for the results given in Figure 3.27(b) [Paw15a].

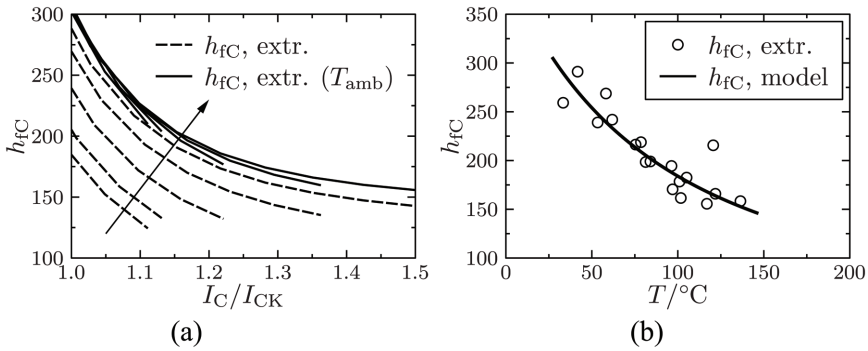
The extraction of  $h_{fE}$  follows the same steps by further including  $h_{f0}\tau_{f0}I_{Tf}$  into (3.56), thus calculating  $h_{fE}$  from

$$h_{fE} = \frac{c_{10}}{I_T} \exp\left(\frac{V_{B'E'}}{V_T}\right) - (Q_{p0} + h_{jEi}Q_{jEi} + h_{jCi}Q_{jCi} + h_{f0}\tau_{f0}I_{Tf}). \quad (3.57)$$

The data in Figure 3.29(a) initially show a strong dependence on  $I_T$  and  $V_{BC}$ , which is caused by self-heating and the temperature dependence of  $h_{fE}$ . After taking into account the temperature dependence according to



**Figure 3.29** (a) Extracted  $h_{FE}$  values at room temperature for different  $V_{BC}$  as indicated by the arrow. (b) Extracted temperature dependence [Paw15a].



**Figure 3.30** (a) Extracted values for  $h_{FC}$  at room temperature for different  $V_{BC}$  as indicated by the arrow. (b) Extracted temperature dependence [Paw15a].

Figure 3.29(b), the bias dependence of  $h_{FE}$  almost vanishes (see solid curves in Figure 3.29(a)).

As the final step,  $h_{FC}$  is extracted analogously by also including  $h_{FE}\Delta Q_{Ef}$  and  $\Delta Q_{Bf}$  into the calculations. Note that  $\Delta Q_{Bf}$  is weighted by 1. Also for  $h_{FC}$ , a strong bias dependence is observed initially, which disappears though after correctly including the effect of self-heating.

### 3.6.3 Physics-Based Parameter Scaling

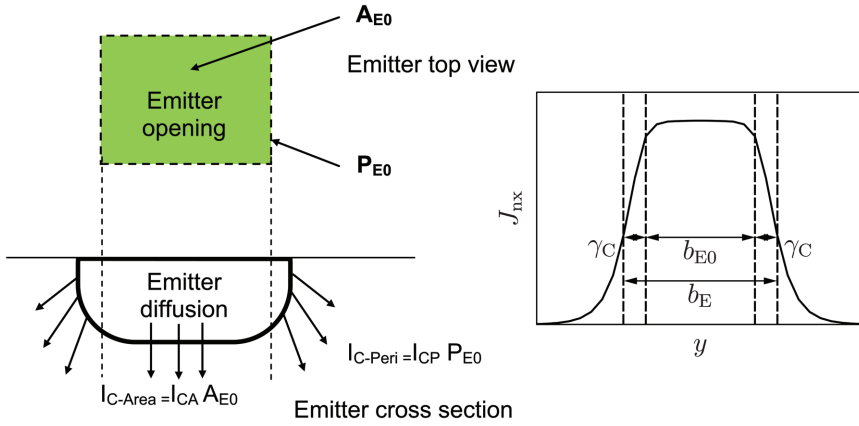
HICUM/L2 has emerged as one of the industry standard bipolar transistor models and was therefore selected as the backbone of the compact transistor modeling strategy in DOTSEVEN. From its first development on in the

1980s, the model has been formulated with geometry scaling capability in mind since this feature has been crucial to achieve the optimum circuit performance for a given process technology. Geometry scaling is fundamentally based on a physics-based model formulation and parameter extraction strategy. Unlike compact MOSFET models, bipolar transistor models do not include scaling equations in their simulator code for several reasons. First, the large variety of possible contact arrangements and structures makes such equations complicated. Second, the accurate calculation of the impact of some effects, such as the geometry dependence of the substrate and thermal coupling, requires the solution of implicit or even differential equations which are difficult to program in simulator-supported description languages including Verilog-A.

Therefore, the development and implementation of HBT geometry scaling formulations is typically left to the foundry or model user. Due to the physics-based formulation of HICUM/L2, its important model parameters can be expressed readily in terms of transistor geometry. Within DOTSEVEN, significant effort was spent on further improving the model's geometry-scaling capabilities for most advanced SiGe HBT structures and for developing reliable geometry-scalable parameter extraction methodologies. Besides enabling the selection of the optimal transistor size for any given circuit application, another benefit is the reduction of the so-called "parameter extraction noise." The latter is a well-known and undesired effect that results in erratic and unpredictable parameter variations with respect to transistor geometry. It occurs when correlated model parameters are extracted on a set of individual transistors by numerical optimization. Geometry-scalable parameter extraction methods have the additional advantage of smoothing random measurement errors and allowing the detection of systematic measurement errors due to, e.g., measurement (equipment) limitations as well as test structure layout and process issues. Finally, scalable models ensure that important model parameters (like the base resistance) behave properly with respect to geometry.

### 3.6.3.1 Standard geometry scaling equation

The most important concept regarding the scaling equations used in conjunction with HICUM/L2 is probably the concept of an *effective* (electrical) emitter area. At low current densities, (i.e., for negligible voltage drops across series resistances), the total collector current can be split into an internal and perimeter portion, each related to a specific emitter region (see Figure 3.31).



**Figure 3.31** The collector current flow in the emitter can be split into an intrinsic portion related to the emitter area and a portion related to the perimeter only. The right picture shows the spatial distribution of the vertical electron current density. Marked are the actual emitter width  $b_{E0}$  as well as the effective emitter width  $b_E$ , calculated from  $b_{E0}$  and  $\gamma_C$  (cf. 3.58, 3.60).

Assuming no impact of collector avalanche or tunneling effects, this graphical concept can be expressed mathematically by

$$I_C = I_{CA}A_{E0} + I_{CP}P_{E0}, \quad (3.58)$$

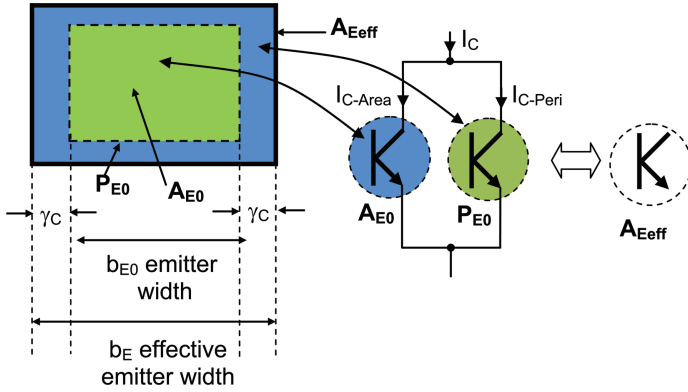
where  $A_{E0} = b_{E0}l_{E0}$  is the actual emitter window area and  $P_{E0} = 2b_{E0} + 2l_{E0}$  is the actual emitter window perimeter<sup>4</sup>, both given by the window opening and interface area of the emitter poly-silicon with the mono-silicon region. Furthermore,  $I_{CA}A_{E0}$  and  $I_{CP}P_{E0}$ , respectively, are the collector components resulting from carrier injection across the emitter window area and window perimeter, respectively. Equation (3.58) can be conveniently reformulated as

$$I_C = I_{CA}A_{E0} \left( 1 + \frac{I_{CP}P_{E0}}{I_{CA}A_{E0}} \right). \quad (3.59)$$

By introducing the process-specific parameter  $\gamma_C$ , defined as the ratio of perimeter-specific to area-specific collector current, (3.59) defines the *effective electrical emitter area*

$$A_E = A_{E0} \left( 1 + \gamma_C \frac{P_{E0}}{A_{E0}} \right), \quad (3.60)$$

<sup>4</sup>Simplified equation neglecting corner contributions and possible corner rounding.



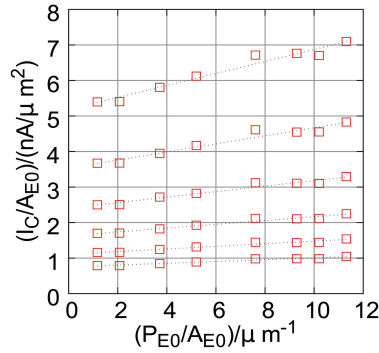
**Figure 3.32** Schematic illustration of the effective emitter area concept. The area and perimeter currents are gathered in a single effective contribution.

which reduces the two current components of (3.58) to a single component with a clearly defined geometry dependence. Therefore, as can be seen from Figure 3.32, this approach allows to represent the internal and perimeter transistor by a single-transistor model having an effective emitter area  $A_E$ . This is obviously advantageous over a two-transistor model approach in terms of computational efficiency and parameter extraction effort. This concept can be easily extended to the modeling of other current components as well as to the charges (and capacitances) of a transistor structure.

According to (3.59), plotting  $I_C/A_{E0}$  versus  $P_{E0}/A_{E0}$  allows to extract the geometry scaling-related parameters  $I_{CA}$  and  $\gamma_C$  from the y intercept and the slope of the curves. This procedure is also known as the P/A (perimeter over area) approach. The application of this concept to experimental data of a DOTSEVEN process in Figure 3.33 displayed the excellent scalability of the collector current. Notice that the use of data from several structures helps averaging out local process variations as compared to performing the extraction from just a single device.

### 3.6.3.2 Generalized scaling equations

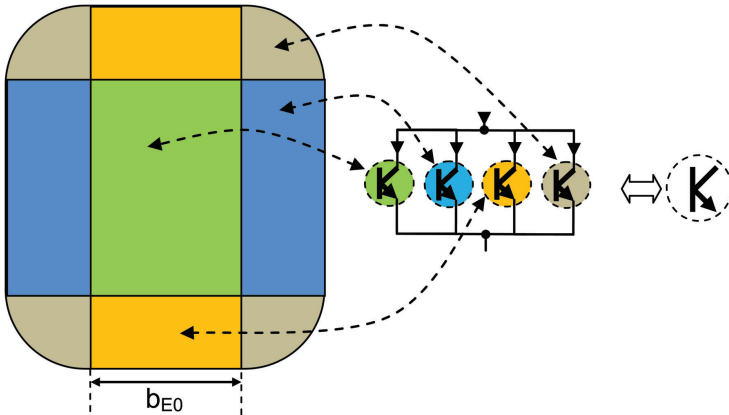
During the various projects (DOTSEVEN, DOTFIVE, RF2THz) deviations from the P/A scaling were observed for some process versions, [Paw13, Paw15b]. It turned out though that such non-standard scaling behavior could be captured by an extension of the standard P/A approach. Figure 3.34 depicts schematically this extension. Again, the goal is to combine the models associated with each lateral region of the transistor into a single model representing a transistor with an effective emitter area  $A_E$ . The extension relies



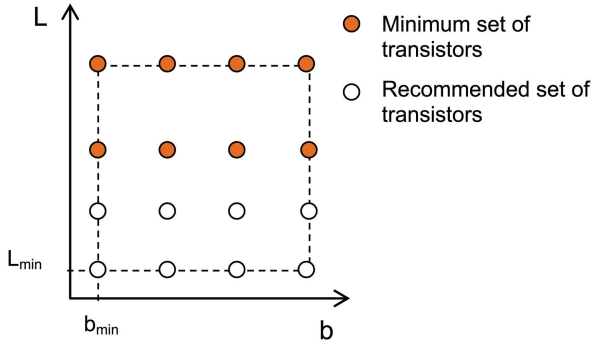
**Figure 3.33** Experimental data of  $I_C/A_{E0}$  versus  $P_{E0}/A_{E0}$  for  $V_{BE} = 0.45\text{--}0.5$  V in steps of 10 mV.  $A_{E0}$  and  $P_{E0}$ , respectively, are the actual emitter window area and perimeter, respectively. The drawn emitter dimensions are  $(0.31, 0.35, 0.4, 0.53, 0.7, 1.2, 2.2) \times 10 \mu\text{m}^2$ . Symbols represent measured data and dashed lines results from linear regression.

on considering the four different components, defined by an injection across the window area, width and length related perimeter junctions, and corner junctions, separately. Obviously, the simple  $P/A$  approach in Figure 3.32 is just a special case of this extended generalized linear scaling approach and is obtained when the specific currents related to the width, length, and corner are merged into a single perimeter related specific current.

In order to properly extract the scalable model parameters for the generalized scaling approach, a matrix of test structure is required with the same set of emitter widths for at least two emitter lengths (see Figure 3.35). From the



**Figure 3.34** Schematic illustration of the generalized effective emitter area concept.



**Figure 3.35** Required matrix of test structures for scalable parameter extraction in the case of the generalized scaling laws.

corresponding measurements, one can obtain a complete set of parameters for each of the different transistors (and associated lateral regions) depicted in Figure 3.34. These parameters then need to be transformed into a set for a single-transistor model. This has been implemented with the help of a Taylor series expansions in the geometry scaling equations for HICUM/L2.

### 3.7 Compact Model Application to Experimental Data

Within DOTSEVEN and related research projects (such as DOTFIVE, RF2THz), HICUM/L2 model parameters were determined from the electrical characteristics measured for many process runs and technology versions. Since the vast amount of data and comparisons cannot be displayed here due to the lack of space, just an overview is given that is based on selected publications<sup>5</sup> and the complete version of HICUM/L2 with all the previously described extensions.

An overview on the overall parameter extraction approach and employed procedures is given in [Paw11], while [Paw14a] highlights the improvements in modeling the transfer current of SiGe HBTs using the extensions described in Section 3.3 and providing a guideline for extracting the new parameters. Very detailed information on both parameter extraction and model comparisons for different process technologies have been given in [Paw15a][Kra15b][Ros17]; these include a large number of DC, AC and

<sup>5</sup>Note that – in contrast to circuit design – the (successful) results of compact modeling can typically not be published for subsequent (and intermediate) process technology versions with improving electrical performance.

large-signal results for a large variety of transistor structures of the technologies developed in different research projects.

A general overview on the modeling results of DOTSEVEN was given in [Paw15b] focussing on a variety of characteristics and operating conditions. The application of the compact model with a focus on decomposing the impact of different physical effects for guiding process technology development has been given in [Paw13], [Kor15], [Paw17a] and [Paw17b].

High-frequency noise, including the correlation between collector current and stored base charge and its generic implementation in circuit simulators, was discussed in [Her12]. There, the applicability of the noise correlation formulation in HICUM/L2 was verified based on the results of the Boltzmann transport equation for frequencies at least up to 500 GHz. Noise measurements at such frequencies are presently impossible so that experimental verifications have been restricted to 50 GHz so far [Her12], [Sak15b], [Sak15]. Here, the accuracy of the model has allowed the decomposition of the various physical noise mechanisms within the transistor, yielding valuable insights into their magnitude and relative importance.

Applications of the compact model with a focus also on circuit results have been demonstrated in [Ard15][Sch16c][Lia17][Sch18b].

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