5

Characterization of Prototypes

5.1 Assessment of Prototype Performance

The assessment of the HIGHTECS prototype parts has covered the following components:

- ASIC in PGA Package
- Hybrid Circuit
- High Temperature PCB for resistors
- HIGHTECS Module

An initial assessment of prototype SiC Transient Voltage Suppressors (TVS) devices in lightning tests has also been carried out.

Long term tests have also been performed on a SOI test chip to identify degradation mechanisms that may occur during the lifetime of the product.

5.1.1 ASIC in PGA Package

90 HIGHTECS ASICs were manufactured in 181 I/O PGA packages to enable functional and environmental tests to be carried out. A high temperature printed circuit board has been designed and manufactured to enable characterisation tests to be carried out.

5.1.2 Functional Tests

Functional testing of the HIGHTECS ASIC assembled in the PGA package has been carried out for the following blocks.

- Bias network
- Single ended to differential converter
- T1 channel measurements
- Band gap voltage
- Strain gauge bridge channels; SG11, SG12, P3

- T4 channel measurement
- Tfo1 and Tfo2
- ADC

The results have shown that the performance of the functional blocks was broadly in line with the expected performance from simulation. The HIGHTECS ASIC as designed has been also shown to function through to the generation of the dual output ARINC 429 data.

The dual outputs from the ARINC 429 databus on the HIGHTECS ASIC were connected to an AIM UK APU 429-4 2 channel transmitter/2 channel receiver to ARINC 429 interface, see Figure 5.1. The data transmitted was then handled by an AIM UK PBA.pro-ARINC429 Database Manager Component. Representative output data are shown in Figure 5.2.

There are several areas of ASIC performance that need further attention, including the ADC, Tfo2 signal, and Nfreq.

5.1.3 Design Changes Implemented for 2nd Version of HIGHTECS ASIC

The work on modifications to the ADC design was undertaken in two stages; the first through modification to the top metallisation layers on 1st version of the HIGHTECS ASIC and the second through a complete re-design of the mask set to incorporate the changes to the ADC and to Tfo2 and Nfreq VHDL code.

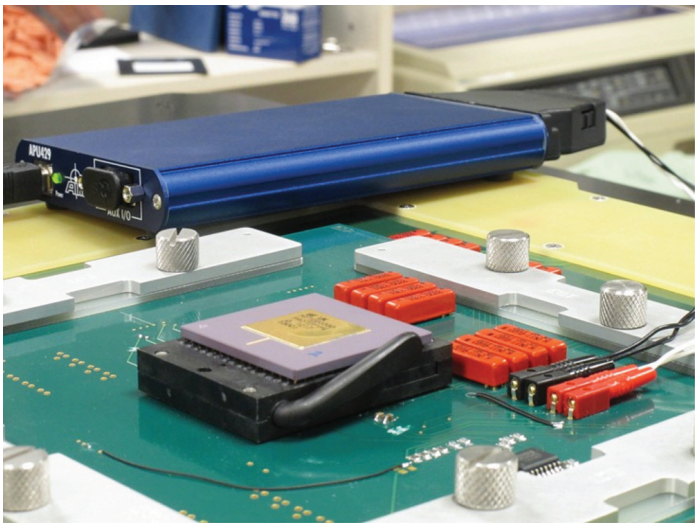

Figure 5.1 HIGHTECS ASIC in PGA package connected to ARINC 429 data reader.

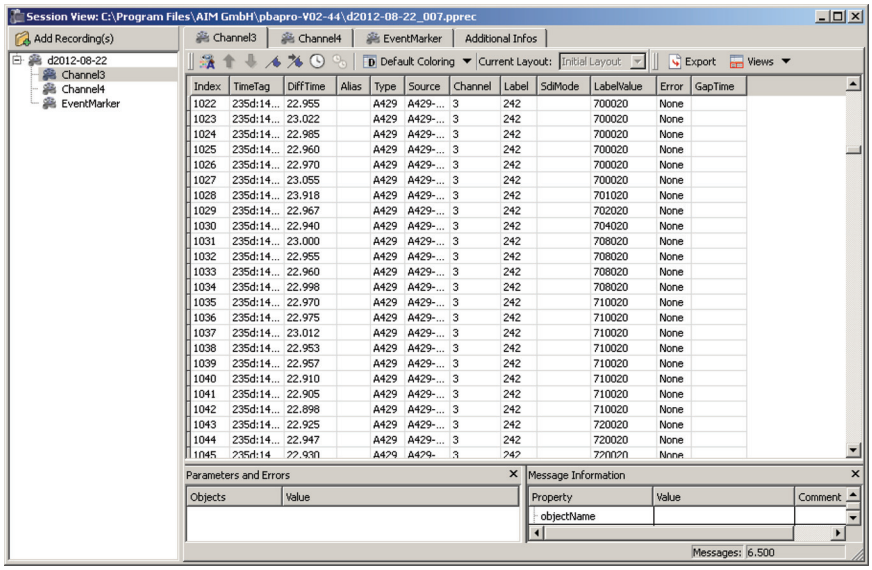

Figure 5.2 ARINC 429 output from HIGHTECS ASIC.

5.1.4 Modification to Top Layer Metallisations on 1st Version of HIGHTECS ASIC

The following changes were implemented in the re-layout of the top layer metallisations on 3 off wafers of the 1st version of the HIGHTECS ASIC held at pre-poly stage:

- Create separate Vrefp and Vrefn inputs of the ADC
- Re-route metallisation lines that were crossing ADC
- Connect DP and DQ to digital pads
- Vdd and Gnd connections of the comparators decoupled from those of the other digital part by direct routing to the pads

The wafers were manufactured at X-FAB and were then wafer probed using the ADC functionality test. The results showed that non-linearity of the ADC output was still apparent at Vdda 5 V and 5.5 V, but was linear at 6 V.

5.1.5 2nd Version of HIGHTECS ASIC

Based on the above results, the 2nd version of the HIGHTECS ASIC was re-designed and manufactured. The ASIC wafer was probe tested and selected samples which passed the within the limits set on the linearity of ADC functionality were assembled into PGA packages. The results of testing the

ASICs in PGA packages at Vdda: 5.5 V for ADC linearity is shown in Figure 5.3.

5.1.6 Environmental Tests

High temperature storage tests (at 200°C and 250°C), temperature cycling and shock/vibration tests have been carried out on selected HIGHTECS ASICs assembled in PGA packages, see Table 5.1. The measurement of analogue I_{dd} has been used as the measure to check on changes in value after testing. All measurements have been performed at room temperature to date.

5.1.7 Characterisation Tests

The characterisation printed circuit board for the HIGHTECS ASIC has been designed and manufactured and is shown in Figure 5.4.

The characterisation board is driven by a FPGA board. The FPGA board has been connected to the characterisation board containing the HIGHTECS ASIC in PGA package and the characterisation board has been placed into either an oven for high temperature testing up to 275°C or a chamber for testing down to –40°C. Characterisation tests have been carried out on the 1st and 2nd version of the ASIC; a couple of example results are presented below.

The change in voltage bandgap against temperature up to 250°C and the effective temperature coefficient are shown in Figure 5.5. SG2 output from the HIGHTECS module at +225°C is shown in Figure 5.6.

5.1.8 Prototype SiC Transient Voltage Suppressors

Prototype SiC Transient Voltage Suppressor (TVS) devices were assembled with copper tags providing the conductor path, as shown in Figure 5.7. These SiC devices can operate at temperatures of at least 200°C, which is above the temperature of commercial Si based lightning protection devices. Preliminary lightning testing has been carried out on these devices, following the procedures of DO-160E.

Pin injection lightning tests following the procedures detailed in RTCA (Radio Technical Commission for Aeronautics)/DO-160E, Section 22.5.1 – Lightning Induced Transient Susceptibility were carried out on the waveforms and levels shown in Table 5.2.

The prototype devices were shown to clamp successfully at the levels and waveforms highlighted in Table 5.2. Further work to assess leakage currents and incorporate the devices into circuits is required.

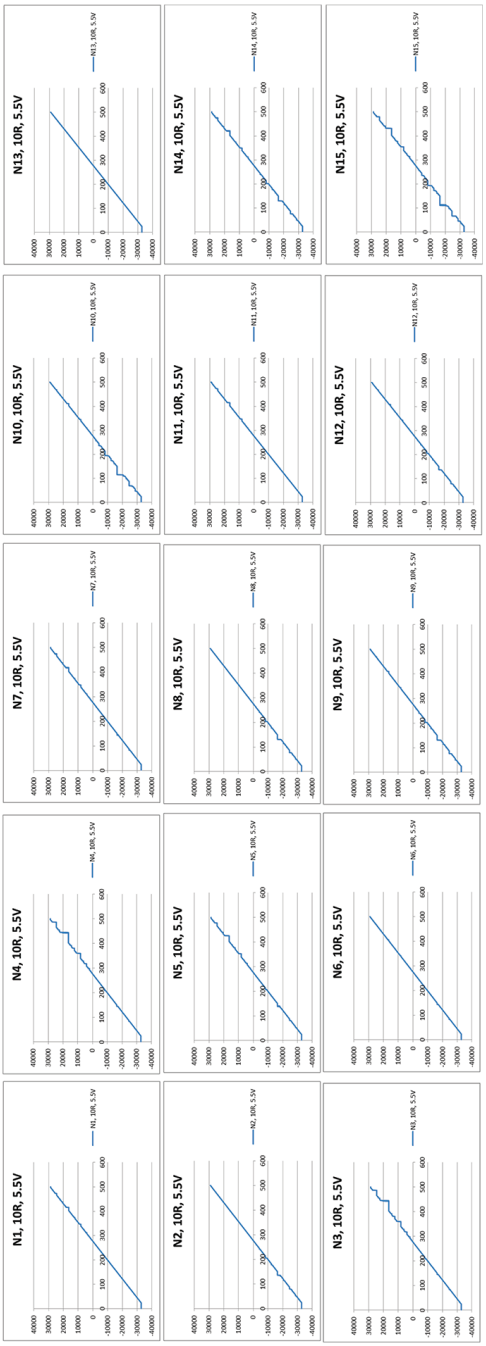

Figure 5.3 ADC linearity plot of 2nd version of HIGHTECS ASIC assembled in PGA packages.

Table 5.1 Summary of environmental tests on HIGHTECS ASIC in PGA package

Environmental Test	Test Condition	Average % Change in I_{dd} Current
High Temperature Storage	8000 hours at 200°C	–2.48%
High Temperature Storage	8000 hours at 250°C	–5.27%
Temperature Cycling	–40°C to +250°C, 375 cycles (min 3 hours at each limit)	–5.39%
Vibration	Random 10–2000 Hz, 0.1 g/Hz^2 3 hours each axis	+1.4%
Vibration and Shock	As vibration test above + Shock 1500 g, 0.5 ms, 5 times, 5 axes	+1.2%

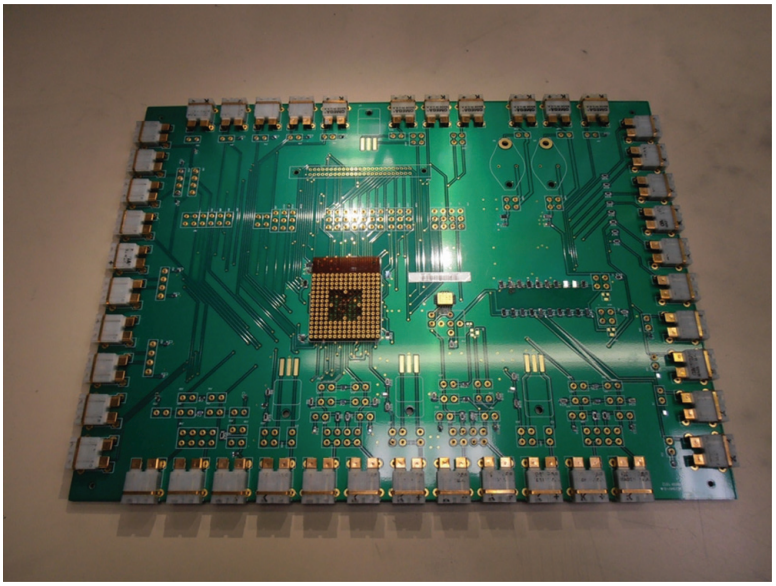

Figure 5.4 Characterisation board for testing of HIGHTECS ASIC in PGA package.

5.2 Testing of SOI Test Chip

Environmental tests have been performed throughout the HIGHTECS project on a SOI test chip fabricated using the same semiconductor process (X-FAB XI10 1 µm) in the manufacture of the HIGHTECS ASIC. This test chip has been assembled into a 48 pin HTCC DIL package and subjected to various environmental tests as described below in Table 5.3 to identify degradation mechanisms that may occur during the lifetime of the product.

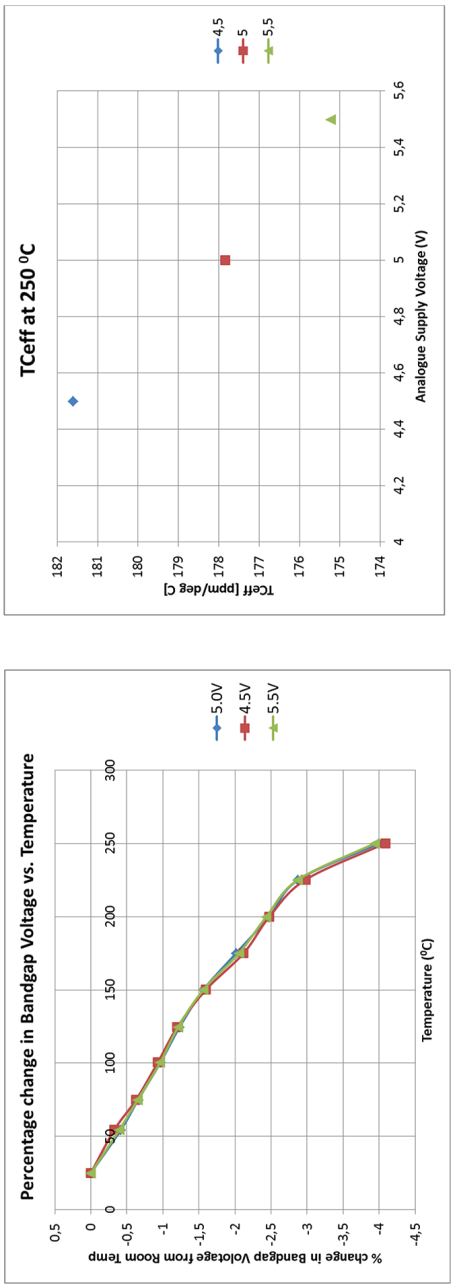

Figure 5.5 Voltage bandgap change with temperature and effective temperature coefficient of 2$^{\mathrm{nd}}$ version of HIGHTECS ASIC.

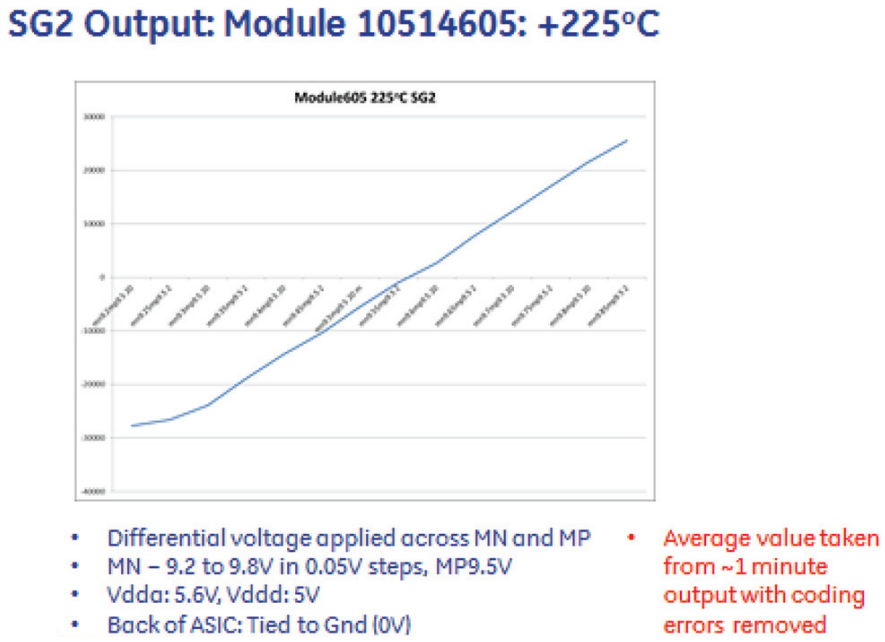

Figure 5.6 Output from SG2 sensor on HIGHTECS module at +225°C.

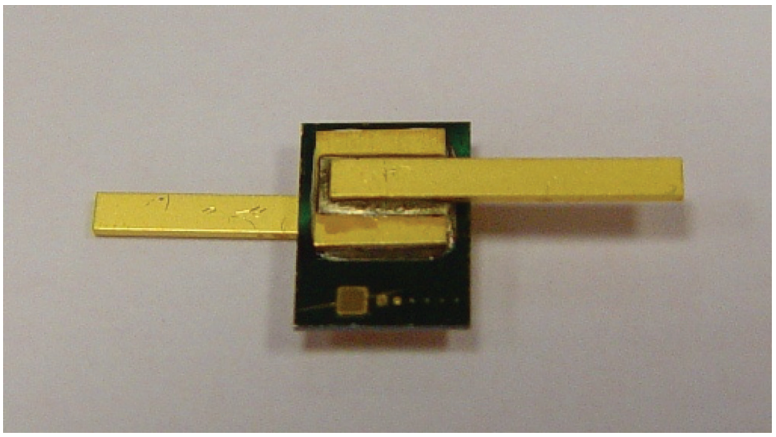

Figure 5.7 Prototype SiC TVS devices with copper tags attached.

5.2.1 High Temperature Storage (250°C)

The main limiting factor on the performance of the SOI test devices assembled in HTCC packages when exposed to temperatures of 250°C for up to 11,000

Table 5.2 Lightning induced transient susceptibility – pin injection tests

	Waveforms		
	3	4	5A
Level	Voc/Isc	Voc/Isc	Voc/Isc
1	100/4	50/10	50/50
2	250/10	125/25	125/125
3	600/24	300/60	300/300
4	1500/60	750/150	750/750
5	3200/128	1600/320	1600/1600

Notes: Voc – peak open circuit voltage (V), Isc – peak short circuit current (A).
For Waveform 3, the frequency was 1 MHz.

Table 5.3 Summary of environmental tests carried out on SOI test chip

Environmental Test	Test Duration	SOI Test Chip Details
High Temperature Storage (250°C)	11088 hours	Batch 1 – Au/TiW metallisation, bond out options 1–6
	7056 hours	Batch 2 – Au/Pd/Ni metallisation, bond out options 1–6
Rapid Thermal Cycling (–40°C to +225°C)	2680 cycles @ ∼5 mins per cycle	Batch 3 – Au/Pd/Ni metallisation, bond out option 7
Vibration (Room Temperature and 200°C)	Resonance Random Sine	Batch 3 – Au/Pd/Ni metallisation, bond out option 7

hours appeared to be the packaging materials used in the assembly process rather than the device itself. There were two principal sources for the degradation; firstly, through the formation of intermetallics between the Au wire bond and the Al metallisation on the bond pad, despite the presence of over bond pad metallisations designed to prevent diffusion of the Al metallisation, and secondly, through the deterioration of the high temperature die attach adhesive within the hermetically sealed package, which caused the formation of whiskers around the bond pads, see Figure 5.8.

In the case of wire bonding, Al-1%Si wire wedge bonded to the Al metallisation on the device was selected as the most stable option. In the case of the die attach, an inorganic Au-Si eutectic solder is recommended to avoid problems of deterioration of organic materials.

5.2.2 Rapid Temperature Cycling (–40°C to +225°C)

The following temperature profiles were provided by Turbomeca:

5.2.2.1 Profile No. 1: 4 × following cycle

- 30 mins, power on, on ground, with stopped engine (Temperature –50°C to +50°C)
- 90 min, power on, in flight with running engine (Temperature 150°C)
- 30 mins, power on, on ground, with stopped engine (Temperature 250°C – approx. 4 mins at 250°C, with 26 mins cooling to ambient)
- 210 mins, power off, on ground, with stopped engine

5.2.2.2 Profile No. 2: 2 × following cycle

- 613 mins, power off, on ground, with stopped engine (Temperature –50°C to +50°C)
- 4 mins, power on, on ground, with stopped engine (Temperature –50°C to +50°C)
- 99 mins, power on, in flight with running engine (Temperature 150°C)
- 4 mins, power on, on ground, with stopped engine (Temperature 250°C)

The number of cycles were calculated for each profile against the specified target operating lifetime of 50,000 hrs. This equates to 8,333 cycles under Profile No. 1 and 4,167 cycles under Profile No. 2. To accelerate this number of cycles in reduced time it was proposed to ramp from the minimum and maximum temperature extremes at the maximum cooling/heating rate with

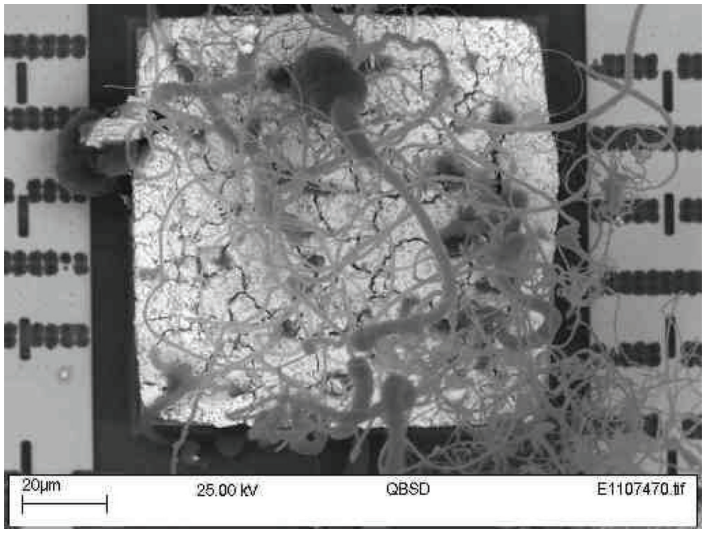

Figure 5.8 SEM picture of unbonded bond pad of adhesive bonded SOI device after 11,088 hours exposure to 250°C showing growth of whiskers.

no dwell time at any temperature. Examples of a full day equivalent running are shown in Figures 5.9 and 5.10 for both profiles.

By having no high temperature dwell any failures due to accumulated strain (e.g. in solder joints and die attach) will be accelerated even more since there will be no opportunity afforded for annealing at temperature.

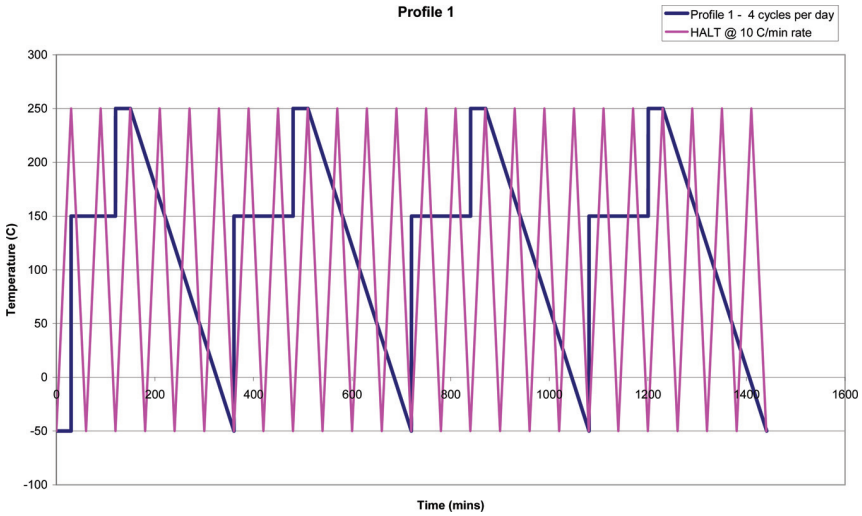

Figure 5.9 Example of full day equivalent running for Profile 1.

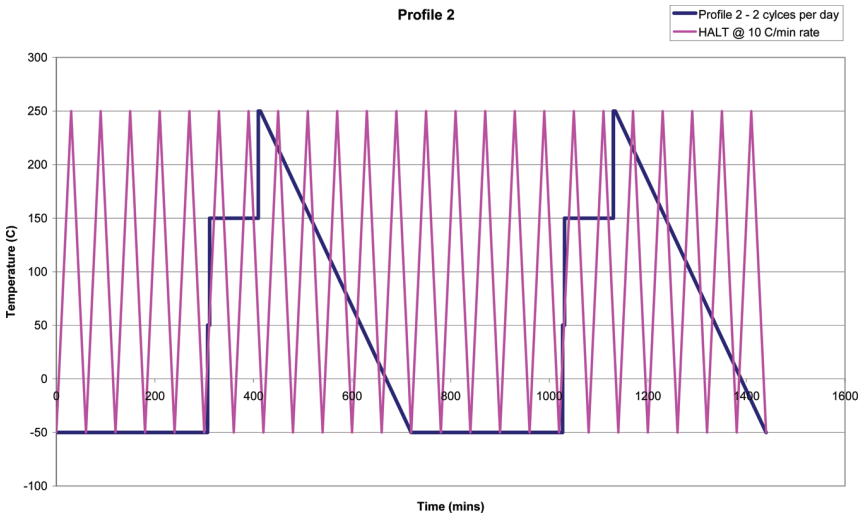

Figure 5.10 Example of full day equivalent running for Profile 2.

Trials have been carried out to assess the performance of SOI test chips after exposure to rapid change of temperature from –40°C to +225°C over a periodic cycle time of ~5 minutes which was the minimum cycle time that could be achieved with the equipment available, see Figure 5.11 for the thermal cycling equipment and Figure 5.12 for the temperature profile.

Packaged SOI test chips were run using rapid thermal cycling and monitoring the gain of an op-amp contained within the device before and after testing.

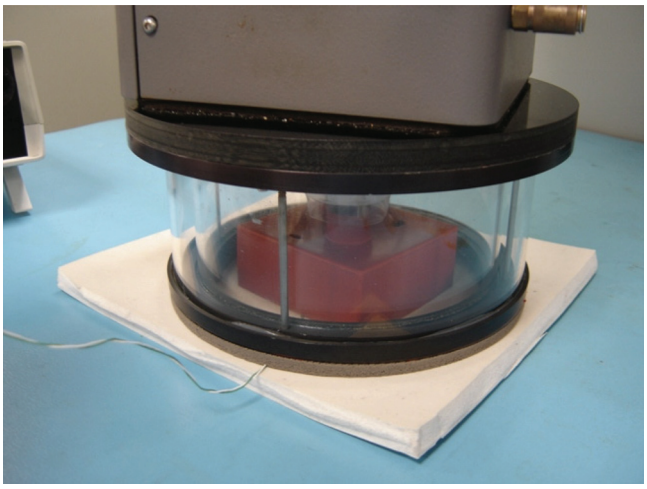

Figure 5.11 Equipment for rapid change of temperature from –40°C to +225°C with 320 second cycle time.

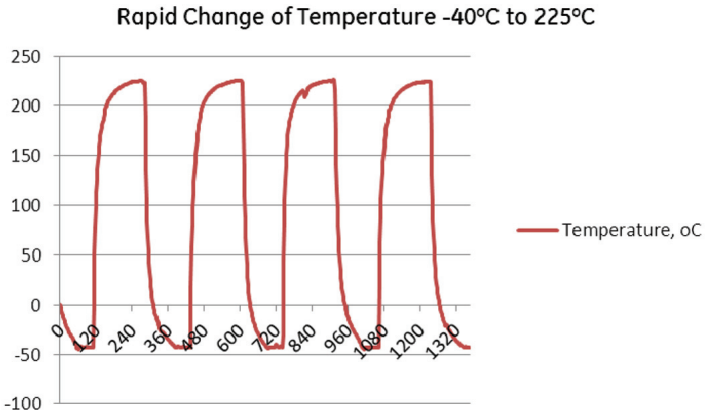

Figure 5.12 Measured temperature profile for rapid change of temperature with 320 second cycle time.

A set of 3 off samples was submitted to 2680 cycles, which represents nearly a third of the expected number of thermal cycles during the lifetime of the component for temperature profile 1 and then tested again. The results showed that little obvious change in op-amp gain was observed. Visual inspection of this sample did not show any obvious degradation.

5.2.3 Vibration (Room Temperature and 200°C)

Vibration testing has been undertaken to ensure that the die attach and wire bonds are not affected by any resonance effects in the sinusoidal vibration modes and random vibrations. The results of the electrical tests after vibration testing showed little difference indicating that conventional vibration testing should not be major concern to the reliability of the assembled ASIC. However vibration testing at temperature may cause additional issues and some additional tests have been carried out to assess this aspect.

SOI test devices with op-amp functional blocks were assembled into HTCC packages with 25 μm diameter Au wire. The gain of the op-amps was measured prior to testing and again after random vibration testing at a temperature of 25°C and 200°C. The results showing the change in op-amp gain at test temperatures of 25°C, 125°C and 250°C indicated that there was little discernible difference in the op-amp gain between the vibration tests carried out at 25°C and 200°C.

5.2.4 Silicon Capacitors

Silicon capacitors supplied by Ipdia were analysed using scanning electron microscopy and energy dispersive X-Ray (EDX) analysis before and after thermal ageing at 250°C. The analysis showed that the capacitors were composed of a monolithic piece of silicon with an Al doped guard ring around the active device, with Au flashed Ni plating as the contact metallisation on the connecting pads. After thermal ageing at 250°C for 24 hours in air, the nickel on the contact metallisation has diffused through the Au metallisation and oxidised to a thickness of ~10 nm of NiO.

10 nF, 100 nF and 1 μF silicon capacitors have been incorporated into the hybrid circuit design. Thermal cycling from –40°C to +250°C of 1206 1 μF silicon capacitors onto alumina substrates using a Ag loaded high temperature conductive adhesive have shown some shorting of the capacitors after less than 10 cycles. An initial investigation has been carried out, which has shown some cracking in the contact metallisation, the dielectric and the silicon. It is believed that the stress caused by thermal cycling of the surface mounted capacitors

onto the alumina substrate results in the cracking of the dielectric beneath the contact pads. Alternative options for assembly have been reviewed and trials have been carried out on wire bonded versions of the Ipdia capacitors, which have shown little variation in capacitance, leakage currents and no occurrence of shorts when subjected to temperature storage at 200°C for >3500 hours and 165 cycles from –40°C to +200°C.

5.3 Functional Tests on Eagle Test Systems

5.3.1 Room Temperature Testing

Details of the testing of the HIGHTECS ASIC assembled in the PGA package for the following functional blocks are presented below.

- Bias network
- Single ended to differential converter
- T1 channel measurements
- Band gap voltage
- Strain gauge bridge channels; SG11, SG12, P3
- T4 channel measurement
- Tfo1 and Tfo2
- ADC

The HIGHTECS ASIC as designed has been shown to function through to the generation of the dual output ARINC 429 data, but there are several areas of ASIC performance that need further attention, including the ADC, Tfo2 signal, Nfreq and the repeatability of the band gap voltage measurement.

ADC: The linearity of the ADC output has been shown to depend on the applied voltage and temperature, with some devices performing better than others. It is believed that impedance on the ADC test pad cells may affect the ADC output. Trials have been carried out to isolate the test pad cells from the circuit using a Focused Ion Beam (FIB), but this did not show any difference in the ADC output. An improvement in the linearity of the ADC output was observed when the digital and analogue V_{dd} were separated by 0.5 V, with 5.5 V on V_{dd} and 6.0 V on V_{dda}. Further simulations have been carried out by IMMS to investigate the effect of supply line resistance, which did not show exactly the same behaviour as the measured devices.

From the initial assessment of ADC performance, it was believed there was some variability in the output of different devices, such that some devices may operate at lower voltages than others. A test program to assess the ADC functionality with a maximum tolerance voltage band of $\pm$0.6 V around the

ADC linear output voltage was developed for probe testing at the wafer level. This program identified a small number of devices (7.5% of the wafer) from the wafer that had an ADC transfer function within the tolerance band at an analogue voltage of 5.5 V and digital output of 5 V. These devices will be assembled into the HIGHTECS hybrid circuits to assess their performance. Although these devices have a functioning ADC, the output may not be linear.

It is believed that a modification to the layout of the connections to and the tracking around the ADC is required to reduce the sensitivity to the applied voltage which will require a new mask set and re-spin of the ASIC.

Tfo1/Tfo2 Signal: Due to an error in the VHDL code, the Tfo2 sensor is a repeat of the Tfo1 sensor and will not show in the ARINC 429 message. This can be corrected by changing the VHDL code, which would require a respin of the ASIC.

Nfreq: In the Nfreq module, there is a requirement for a Nfreq pulse before the state machine can change state. This works for frequencies below the minimum, but the state machine becomes stuck of the Nfreq frequency is zero. A change in the VHDL code to overcome this effect is required.

Band Gap Voltage: The repeatability of the band gap voltage measurement appears to be related to the test equipment set up and the application of power resources to the component during testing.

The dual outputs from the ARINC 429 databus on the HIGHTECS ASIC were connected to an AIM UK APU 429-4 2 channel transmitter/2 channel receiver to ARINC 429 interface, see Figure 5.13. The data transmitted

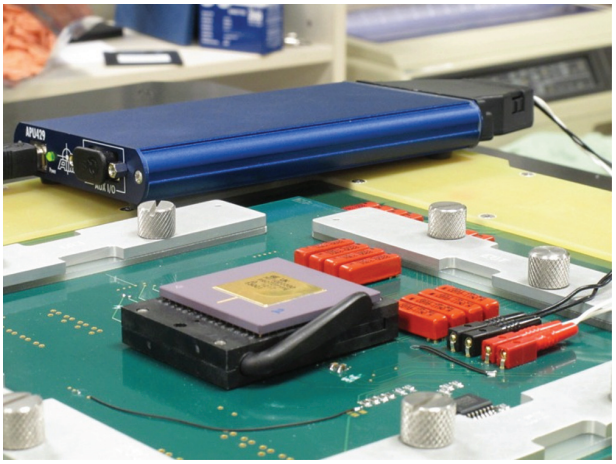

Figure 5.13 HIGHTECS ASIC in PGA package connected to ARINC 429 data reader.

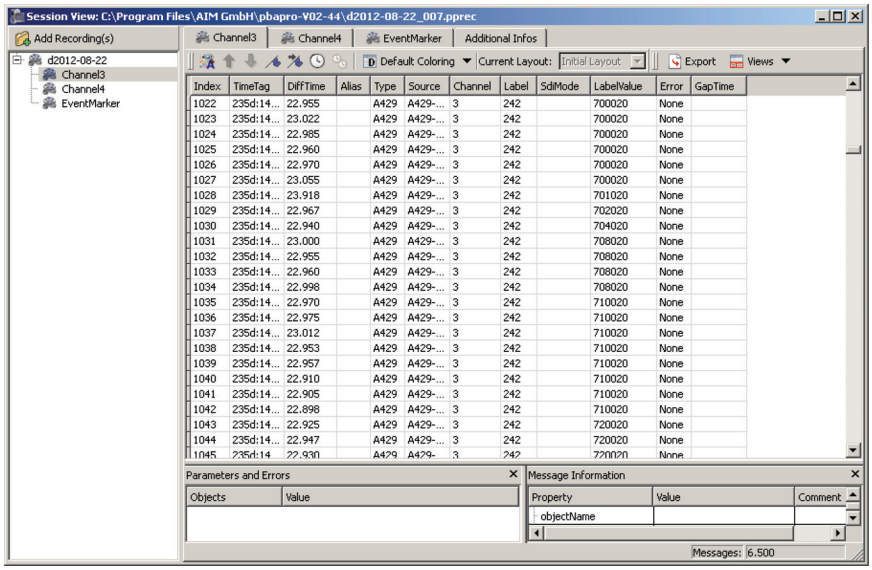

Figure 5.14 ARINC 429 output from HIGHTECS ASIC.

was then handled by an AIM UK PBA.pro-ARINC429 Database Manager Component. Representative output data are shown in Figure 5.14.

5.3.2 High and Low Temperature Testing

High and low temperature functional testing of the HIGHTECS ASIC is to be carried out after the completion of the functional tests at room temperature.

5.3.3 Environmental Tests

5.3.3.1 High temperature storage (200°C and 250°C)

High temperature storage tests have been carried out on selected HIGHTECS ASICs assembled in PGA packages. The measurement of analogue I_{dd} has been used as the measure to check on changes in value after testing. All measurements have been performed at room temperature to date. The results for 200°C storage and 250°C storage up to 8000 hours are presented in Tables 5.4 and 5.5 respectively.

Scanning Electron Microscopy (SEM) of thermally aged samples at 200°C and 250°C for 8000 hours has been carried out, which showed little degradation of the HIGHTECS ASIC, the die attach, the wire bond interconnections and the PGA package.

Table 5.4 Temperature storage tests at 200°C on HIGHTECS ASIC in PGA package

		Analogue I_{dd}, mA			
Sample No	Storage Test Temperature	0 Hours	360 Hours	2100 Hours	8000 Hours
74	200°C	10.15	10.35	10.10	10.00
75	200°C	10.26	10.05	9.95	9.91
76	200°C	10.33	10.31	10.33	10.30
77	200°C	10.34	10.29	10.12	9.93
78	200°C	10.25	10.38	10.02	9.91
79	200°C	10.05	10.17	9.99	9.86
80	200°C	10.50	10.44	10.46	10.37
81	200°C	10.25	10.20	10.19	10.10
82	200°C	10.38	10.38	10.20	10.17
83	200°C	10.26	10.37	10.19	10.13
84	200°C	10.35	10.34	9.98	9.95
85	200°C	10.19	10.21	9.89	
86	200°C	10.35	10.34	10.05	10.03
87	200°C	10.27	10.28	9.87	9.77
88	200°C	10.26	10.17	9.77	

Table 5.5 Temperature storage tests at 250°C on HIGHTECS ASIC in PGA package

		Analogue I_{dd}, mA			
Sample No	Storage Test Temperature	0 Hours	260 Hours	2000 Hours	8000 Hours
52	250°C	10.35	10.33	9.83	9.96
53	250°C	10.09	10.12	9.75	9.38
54	250°C	10.02	9.86	9.81	9.58
55	250°C	10.17	10.10	9.92	9.89
56	250°C	10.62	10.39	10.24	9.58
57	250°C	10.33	10.34	9.81	
58	250°C	10.23	10.18	9.74	

5.3.3.2 Temperature cycling (–40°C to +250°C)

Temperature cycling tests have been carried out on selected HIGHTECS ASICs assembled in PGA packages. The measurement of analogue I_{dd} has been used as the measure to check on changes in value after testing. All measurements have been performed at room temperature to date. The results are presented in Table 5.6.

Scanning Electron Microscopy (SEM) of thermally cycled samples from –40°C to 250°C for 375 cycles has been carried out, which showed some cracking of the die attach material, see Figure 5.15.

Table 5.6 Temperature cycling tests from –40°C to 250°C on HIGHTECS ASIC in PGA package

		Analogue I_{dd}, mA			
Sample No	Temperature Cycling Range	0 Cycles	10 Cycles	100 Cycles	375 Cycles
59	–40°C to 250°C	10.07	10.21	9.95	9.54
60	–40°C to 250°C	10.03	10.06	9.74	
61	–40°C to 250°C	9.95	10.09	9.71	
62	–40°C to 250°C	10.39	10.44	10.23	
63	–40°C to 250°C	10.17	10.38	9.96	9.58
64	–40°C to 250°C	10.15	10.15	9.77	9.68
65	–40°C to 250°C	10.22	10.16	9.81	
Average Percentage Change in Analogue I_{dd} Current				–2.56%	–5.39%

Notes on test conditions: Samples stored for at least 3 hours at each temperature extreme within maximum transfer time of 30 minutes.

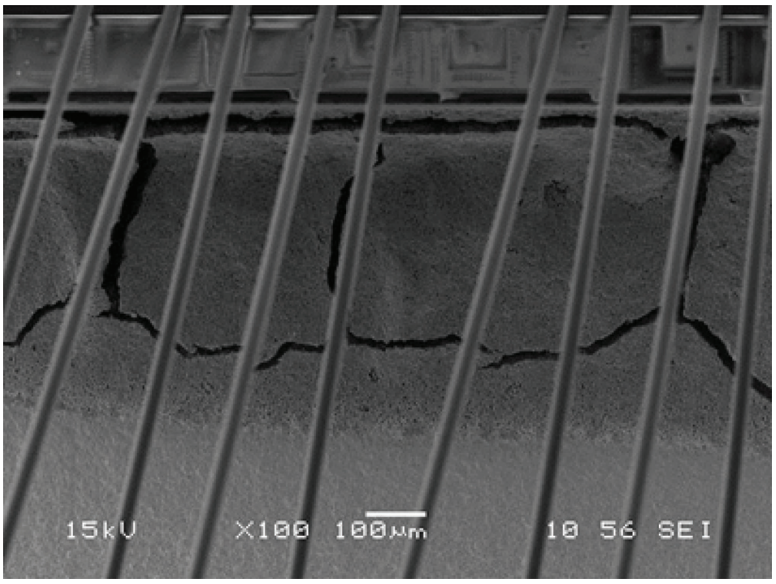

Figure 5.15 Cracking of die attach material after 375 cycles from –40°C to +250°C.

5.3.3.3 Vibration/Shock

Vibration and shock tests have been carried out on selected HIGHTECS ASICs assembled in PGA packages. The measurement of analogue I_{dd} has been used as the measure to check on changes in value after testing. The results are presented in Table 5.7.

Table 5.7 Vibration and shock tests on HIGHTECS ASIC in PGA package

		Analogue I_{dd}, mA		
Sample No	Test	Before	After	% Change
67	Vibration and Shock	10.36	10.52	+1.5
68	Vibration and Shock	10.30	10.51	+2.0
69	Vibration and Shock	10.10	10.27	+1.6
70	Vibration and Shock	10.44	10.42	–0.2
71	Vibration	10.25	10.41	+1.6
72	Vibration	10.21	10.27	+0.6
73	Vibration	10.34	10.55	+2.0

Notes on test conditions:
Vibration test: Random 10–2000 Hz, 0.1 g/Hz^2, 3 hours each axis.
Shock test: 1500 g, 0.5 ms, 5 times, 5 axes.

5.3.3.4 Testing of HIGHTECS hybrid circuit and high temperature PCB containing resistors

Boxes for testing of the HIGHTECS hybrid circuit and HIGHTECS module have been designed and manufactured, as shown in Figures 5.16–5.18. The boxes have been designed to test the various inputs on the HIGHTECS circuit. The hybrid circuit can be mounted onto the socket and tested prior to final assembly.

The output from a HIGHTECS hybrid circuit (Hybrid Serial Number 10511832) with all sensor inputs open circuit connected to the ARINC 429 Bus Monitor User Interface is presented in Figure 5.19. The red LEDs are all indicating open circuit errors as expected. The Tfo2 signal has no error

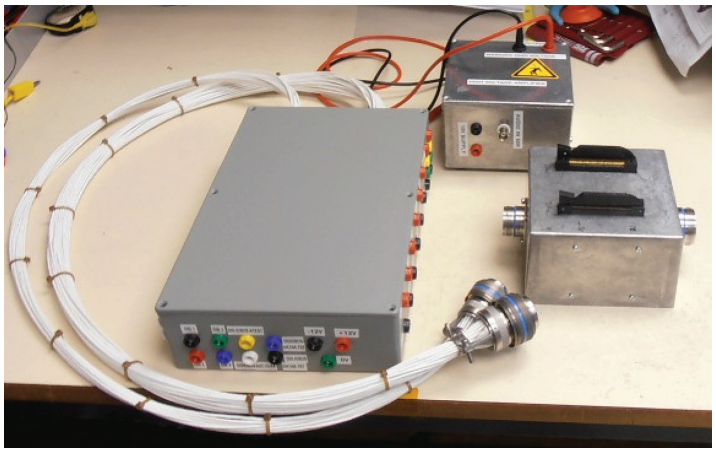

Figure 5.16 Test Box for HIGHTECS hybrid circuit and module.

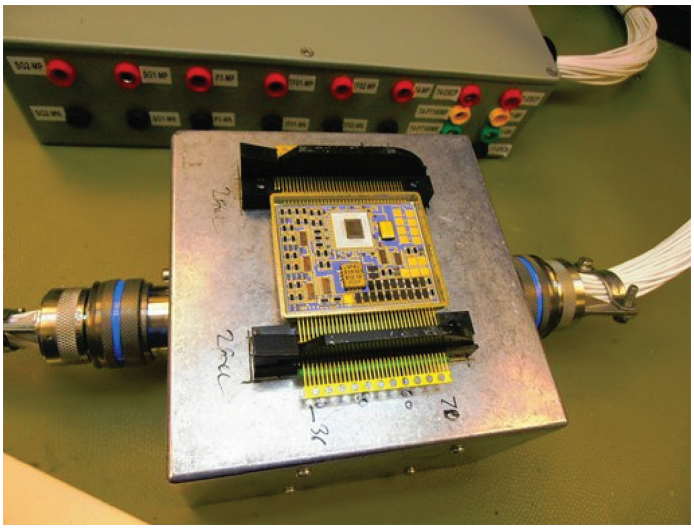

Figure 5.17 Test of HIGHTECS hybrid circuit.

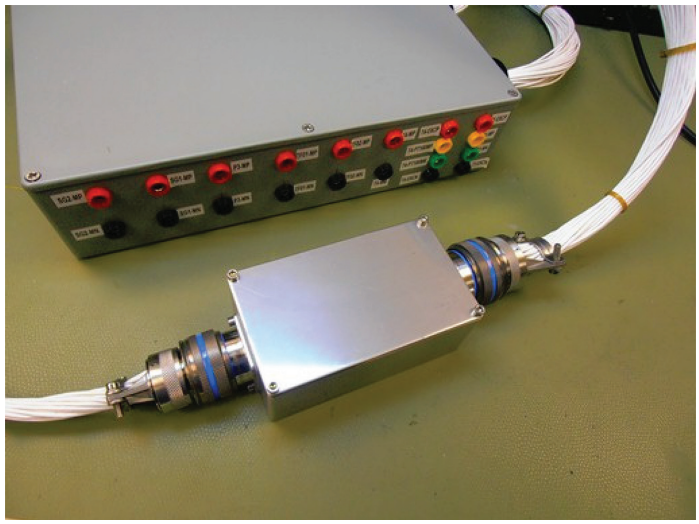

Figure 5.18 Test of HIGHTECS module.

message, which was as expected as no ARINC messages were generated for this sensor. T4 signal is indicating an open circuit. Nfreq and Qfreq are indicating "overrange" and DIN sensors are all showing open circuit as expected.

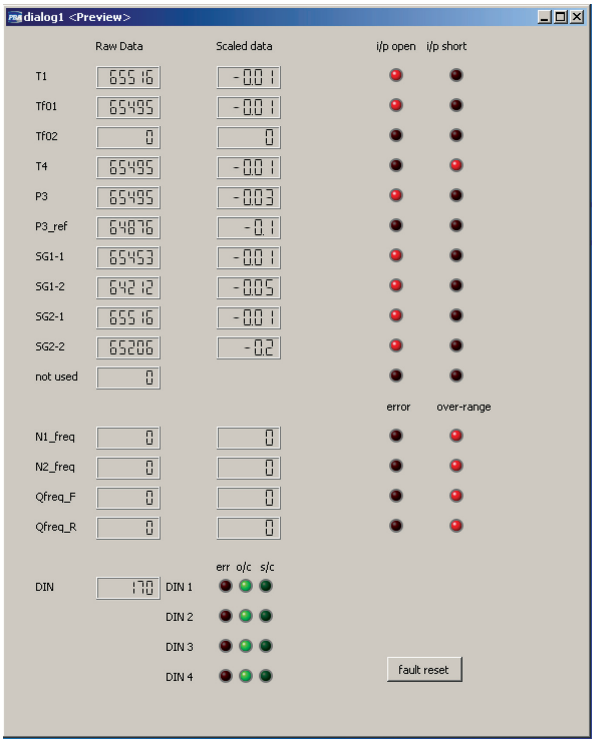

Figure 5.19 Output from ARINC 429 monitor from HIGHTECS hybrid.

Oscillations of the ARINC 429 signal were observed on most of the samples, which required additional capacitors on the input side of the supply regulators and the +ve and –ve power supplies needed to be applied simultaneously to avoid an overload effect on the hybrid circuit.

Tests have been carried out on the HIGHTECS hybrids to identify which connections are needed to provide an output on the ARINC 429 reader. The tests have shown that the following connections need to be applied to the HIGHTECS hybrid circuit:

- ADCSTARTX and ADCRESNX tied to Vdd
- ATEST, ADC_CLKX and ASEX0-ASELX3 tied to GND

The outputs from the TFo1 analog sensors on the ARINC429 reader are shown in Figure 5.20.

The results indicated that the analog sensors were working but the results were affected by the non-linearity in the ADC performance, which caused the spurious readings.

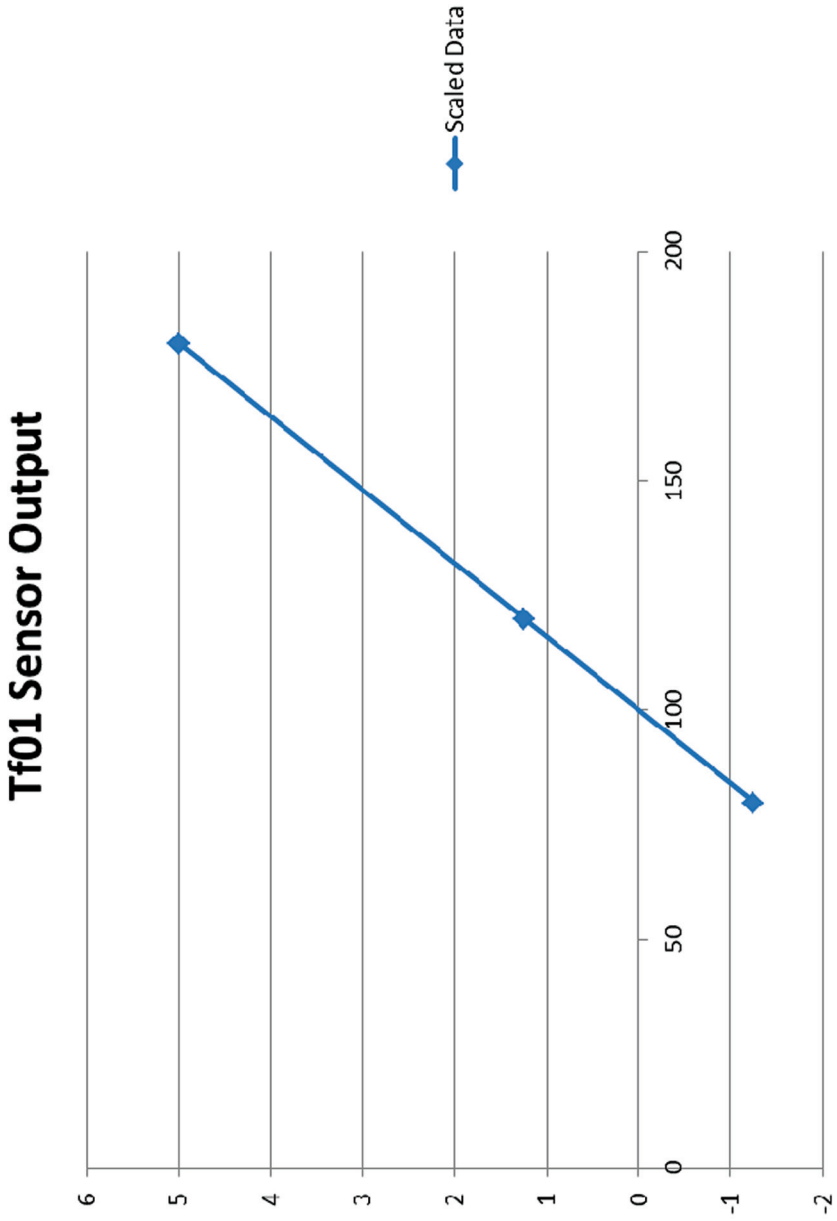

Figure 5.20 Tfo1 sensor output from HIGHTECS hybrid.

Testing of the Qfreq sensor was carried out using two pulse generators that were set up to provide two pulses, see Figure 5.21. The graph showing the response against frequency is shown in Figure 5.22, where the measured accuracy was better than 0.03% at room temperature.

The output from a representative HIGHTECS hybrid circuit with all sensor inputs open circuit connected to the ARINC 429 Bus Monitor User Interface is presented in Figure 5.19. The red LEDs are all indicating open circuit errors as expected. The Tfo2 signal has no error message, which was as expected as no ARINC messages were generated for this sensor. T4 signal is indicating an open circuit. Nfreq and Qfreq are indicating "overrange" and DIN sensors are all showing open circuit as expected.

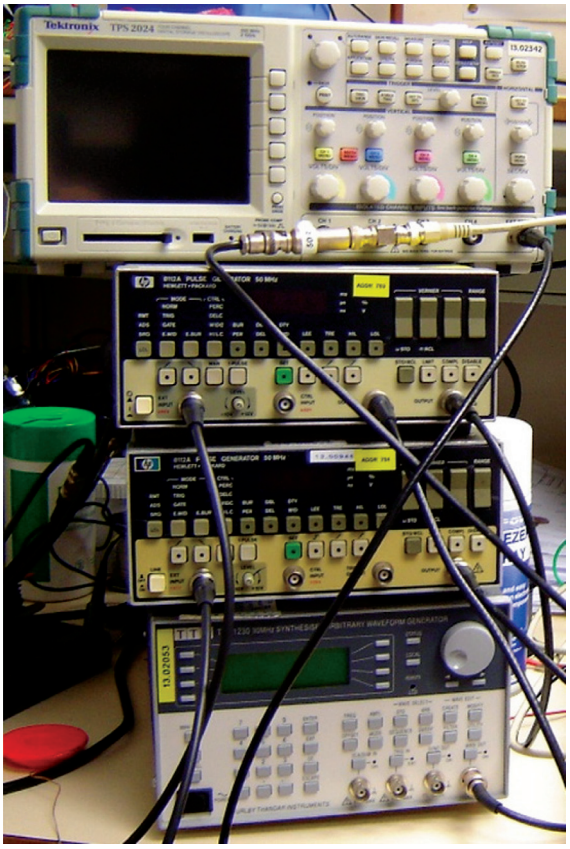

Figure 5.21 Pulse generators used for testing of Qfreq sensor.

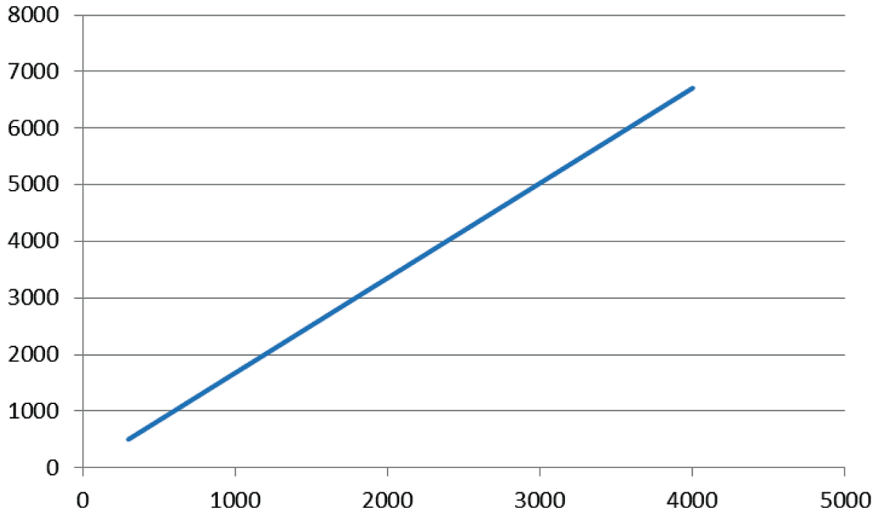

Figure 5.22 Qfreq sensor output against input frequency at room temperature.

Further work on the HIGHTECS hybrid to identify the signals required to operate the ADC correctly was undertaken, which produced near-expected outputs for the linear sensors and the frequency sensors. One HIGHTECS hybrid circuit (10514605) was assembled into a complete module and the unit has been shown to function from –40°C to +225°C, with the linearity of the SG2 sensor output improving as the temperature increases above ambient, see Figure 5.19.