

4

Design and Characterization of HIGHTECS Signal Channels and Building Blocks

4.1 Operational Amplifiers

Three operational amplifiers with class-AB output stages were designed during HIGHTECS: one with a PMOS input stage, one with a NMOS input stage and one with a rail-to-rail input stage [1]. The rail-to-rail version is presented in Figure 4.1. The opamps have been used in the signal conditioning blocks as well as the bias block for stable generation of currents and voltages, and these, in turn, have been used to bias the strain, temperature, and frequency channels for signal conditioning.

The simulated performance of the rail-to-rail opamp across corners is presented in Table 4.1. While the opamps were not measured directly, their performances were indirectly evaluated in the signal conditioning instrumentation amplifiers and in the voltage to voltage and voltage to current converters in the bias block. These bias and signal conditioning channels were measured and the results will be shown in the measurement results section.

Table 4.1 Rail-to-Rail opamp corner simulation results

Specification	Min	Nom	Max	Units
Supply Voltage	4.5	5	5.5	V
Bias Current	30	55	70	μ A
Current Consumption		586	860	μ A
Temperature	-60	27	+225	$^{\circ}$ C
Input Voltage	0.5	2.5	4.5	V
Load Current	-100	50	100	μ A
Capacitive Load	0	1.5	3	pF
DC open-loop Gain	64	106	113	dB
3-dB BW in Voltage-follower Config.	2.6	9.94	23.3	MHz
Phase Margin	52	72.78	99	$^{\circ}$
Gain Margin	5.8	14.2	40	dB

4.1.1 Rail-to-Rail OpAmp

4.1.1.1 Schematic diagram

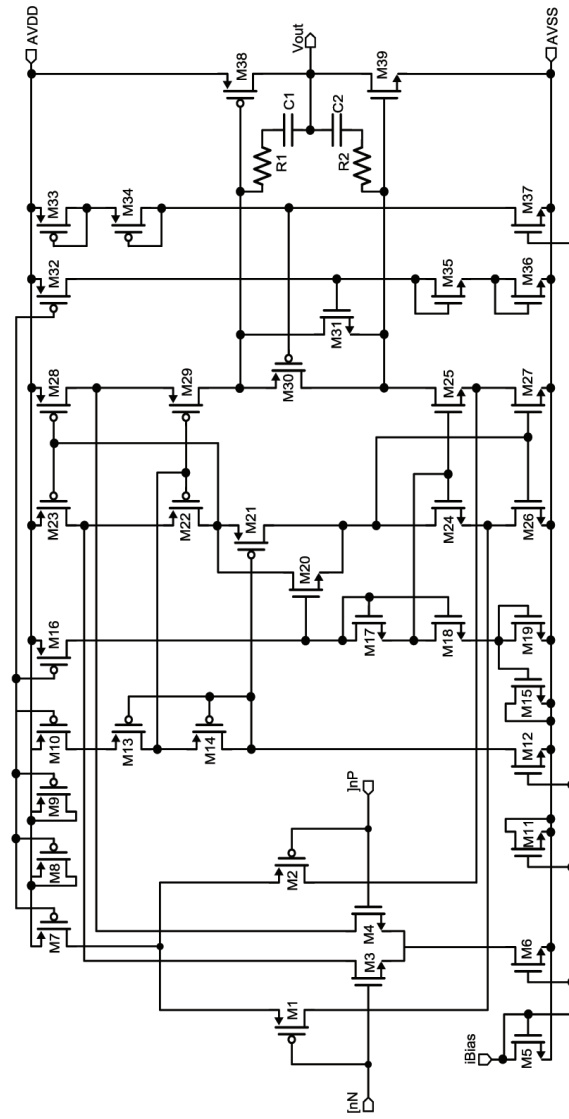


Figure 4.1 Rail-to-Rail Class-AB Output Stage Opamp Schematic.

4.1.1.2 Layout

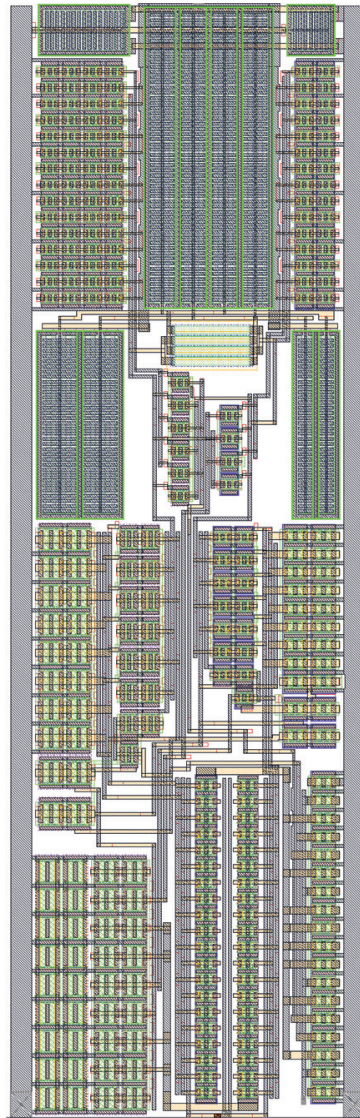


Figure 4.2 Rail-to-Rail Class-AB Output Stage Opamp Layout.

4.1.1.3 Simulation results

The OpAmp model for simulation includes layout capacitive and resistive parasitics. The design was simulated over 505 corners defined as combination of following parameters:

```
DesignVar = {'CL' '0p' '3p' 'x' 'x' 'x'; ...
             'Vdc' '0.5' '2.5' '4.5' 'x' 'x'; ...
             'Iref' '30u' '70u' 'x' 'x' 'x'; ...
             'IL' '-100u' '0u' '100u' 'x' 'x'; ...
             'temp' '-60' '225' 'x' 'x' 'x'};

ModelSection = {'bsim3v3.scs' 'cap.scs' 'res.scs' 'dio.scs'; ...
                'tm' 'tm' 'tm' 'tm'; ...
                'wp' 'wp' 'wp' 'tm'; ...
                'wp' 'ws' 'ws' 'tm'; ...
                'ws' 'wp' 'wp' 'tm'; ...
                'ws' 'ws' 'ws' 'tm'; ...
                'wo' 'wp' 'wp' 'tm'; ...
                'wz' 'wp' 'wp' 'tm'};
```

4.1.2 PMOS-input OpAmp

Several operational amplifiers with class-AB output stages [2] were designed: one with a PMOS input stage, one with a NMOS input stage and one with a rail-to-rail input stage [1, 3]. The PMOS input stage class-AB output stage version presented in Figure 4.3 have been used inside the instrumentation amplifier (IA) for the strain gauge signal conditioning channel and in the Single Ended to Differential Converter (SEDC) placed before the analogue to digital converter (ADC).

The simulated performance of the PMOS opamp across process, voltage and temperature (PVT) variation is presented in Table 4.2. The opamp has a PMOS input stage M_1 , M_2 , allowing common-mode input voltage down to the negative rail. Class-AB control is provided by M_{19} and M_{23} devices. The cascode mirror M_{15} , M_{16} , M_{20} , M_{21} is biased by M_{10} – M_{12} while the cascode mirror M_{13} , M_{14} , M_{17} , M_{18} is being biased by M_5 – M_7 . A constant operating point over the -40°C to 225°C temperature range was obtained based on the ZTC and “ g_m/I_D ” methodologies [4] and on the corresponding constant

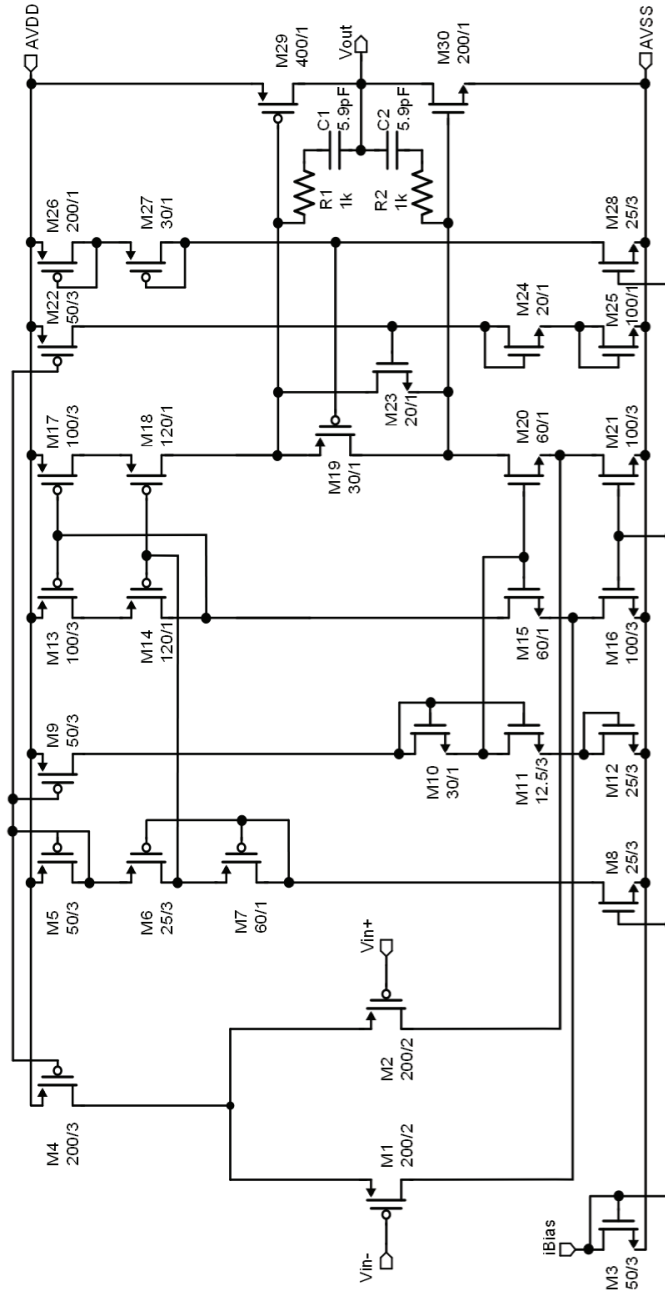


Figure 4.3 Schematic of the PMOS input opamp with class-AB output stage.

Table 4.2 Corner simulation results of the PMOS input opamp with class AB output stage

Specification	Min	Nom	Max	Units
Supply Voltage	4.5	5	5.5	V
Bias Current	30	55	70	μA
Current Consumption	221	459	804	μA
Temperature	-60	27	+225	$^{\circ}\text{C}$
Input Voltage	0.5	2.5	3	V
Load Current	-100	50	100	μA
Capacitive Load	0	1.5	3	pF
DC open-loop Gain	70	111	114	dB
3-dB BW in Voltage-follower Config.	3	5.88	20	MHz
Phase Margin	57	71.82	101	$^{\circ}$
Gain Margin	9	13.19	37	dB
Systematic offset voltage	-2.4	0.15	1.2	mV

bias current. Frequency compensation is obtained using *Miller* capacitors C_1 and C_2 . The *Miller* capacitors determine the unity-gain frequency ω_0 of the opamp as given by:

$$\omega_0 = \frac{g_{m2}}{C_{Miller}}, \quad (4.1)$$

where g_{m2} is the transconductance of the input stage and C_{Miller} is equal to the C_1 and C_2 capacitors. Due to constant operating point, the transconductance reduces with temperature proportionally for all transistors, such that the poles and zeros keep their relative position. R_1 and R_2 have been chosen with the lowest temperature coefficient to ensure frequency stability over temperature. All devices were laid out as interdigitated devices to minimize the impact of thermal gradients. While the PMOS opamp was not measured directly, its performances were indirectly evaluated in the signal conditioning IA and in the SEDC. The signal conditioning channel and the SEDC were measured, and the results will be shown in Section 4.6.4.

4.1.3 NMOS-input OpAmp

An NMOS input class-AB operational amplifier was designed based on [2, 5, 6]. The schematic of the *OP2* and *OP3* operational amplifiers from Figure 4.58 is presented in Figure 4.4. The minimum input voltage should not be below $V_{in_{min}} = V_{tn1} + V_{ov1} + V_{ov4}$ volts, where V_{tn1} is the threshold voltage of M_1 and V_{ov1} and V_{ov4} are the overdrive voltages of M_1 and M_4 , respectively. $V_{in_{min}}$ almost doubles with the change of temperature from 200°C down to -55°C . *OP2* is driven by the source follower (M_5) comprising an additional diode (D_1) in the current branch to provide the

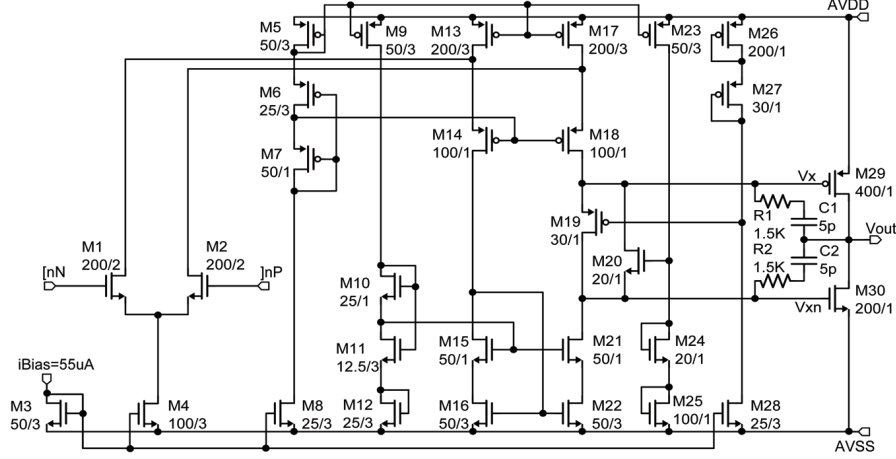


Figure 4.4 Circuit schematic, device sizes and bias current of the NMOS input class AB output stage opamp.

necessary minimum voltage biasing for the *OP2* opamp, thus keeping all transistors of the input differential pair in saturation at all temperatures within the specified range. Cascode devices M_{15} and M_{21} are biased from the simplified Sooch current mirror $M_{10} - M_{11} - M_{12}$. Based on the ZTC and “ g_m/I_D ” methodologies [4] and on the corresponding constant bias current, a constant operating point over the -40°C to 225°C temperature range was achieved. This also guarantees that the transconductance reduces with temperature proportionally for all transistors, such that the poles and zeros keep their relative position. For a value of $I_{dso} = 5.5 \cdot 10^{-7}$ A, the input transistors M_1 and M_2 have been biased and sized for a value of $g_m/I_D = 9.6 \text{ V}^{-1}$ at 27°C and a value of 6.14 V^{-1} at 225°C , similar with values reported in [4]. The measured potential shift with temperature at the output of the class AB opamp connected in unity gain configuration is from 2.5 mV at 200°C to 6 mV at 250°C , similar with the results reported in [4]. The cascode voltage tracks the threshold and overdrive voltage change over temperature, thus properly biasing M_{15} and M_{21} at extreme temperatures. In order to guarantee the opamp stability over the specified temperature range, a bias current of $i_{Bias} = 55 \mu\text{A}$ was used. The output class AB stage can provide currents of $\pm 100 \mu\text{A}$, which is several times larger than the nominal quiescent current. The measured output impedance of $Z_{out} = 586 \Omega$ at 225°C shows that the Early voltage defining the output conductance at fixed bias current remains fairly constant.

Table 4.3 Process variation

CAP	RES	DIO	MOS
TM	TM	TM	TM
WP	WP	WP	WP
WS	WS	WS	WP
WP	WP	WP	WS
WS	WS	WS	WS
WP	WP	WP	WO
WP	WP	WP	WZ

Table 4.4 PVT corner simulation results of the NMOS input class AB output stage opamp. Process variation corners are presented in Table 4.3

Specification	Min	Nom	Max	Units
Supply	4.5	5	5.5	V
Bias Current	30	55	70	μA
Temperature	-60	27	+225	$^{\circ}\text{C}$
Current Consumption	200	450	730	μA
Input Voltage	1.9	2.5	4.5	V
Load Current	-100	0	100	μA
Capacitive Load	0	1.5	3	pF
DC open-loop Gain	66	107	116	dB
Unity gain BW	2	8.4	18	MHz
Phase Margin	64	84.9	115	$^{\circ}$
Gain Margin	10.9	22.11	35	dB
Systematic offset voltage	0.35	0.5	9.4	mV

Simulation results of the NMOS input opamp under a variety of process variation (Table 4.3), supply voltage and temperature (PVT) corners are shown in Table 4.4, where its robustness is evident. In Table 4.3, the acronyms TM, WP, WS, WO and WZ are denoting the process variation for typical mean, worst power, worst speed, worst one and worst zero, respectively. The three input opamp ($OP1$) from Figure 4.58 is used to control the charging PMOS device of the peak detector. The voltage at the input transistor M_{11} sets the minimum level for which the peak detector starts tracking the peaks of input signal. $OP1$ schematic is presented in Figure 4.5. With the exception of M_{11} , $OP1$ from Figure 4.58 has the same bias current, devices sizes and gain as $OP1$ from Figure 4.57.

4.2 Bandgap Reference Generator

The temperature stable bandgap reference voltage generator shown in Figure 4.6 is based on the work in [7]. It is a symmetrically matched

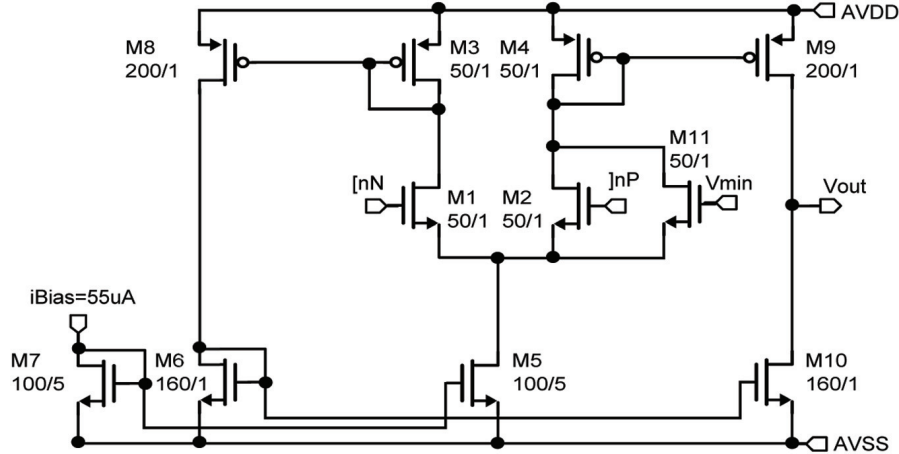


Figure 4.5 Circuit schematic, device sizes and bias current of the 3 input opamp.

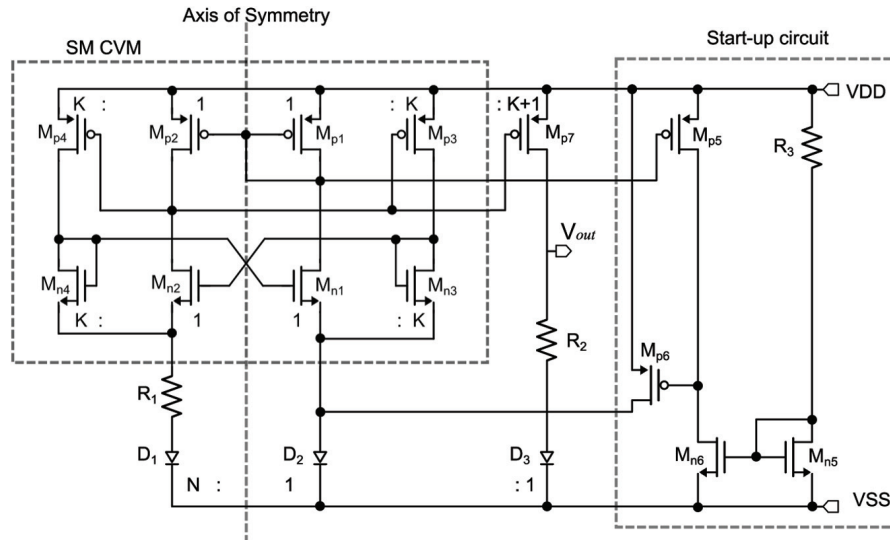


Figure 4.6 Symmetrically matched current-voltage mirror to generate V-reference.

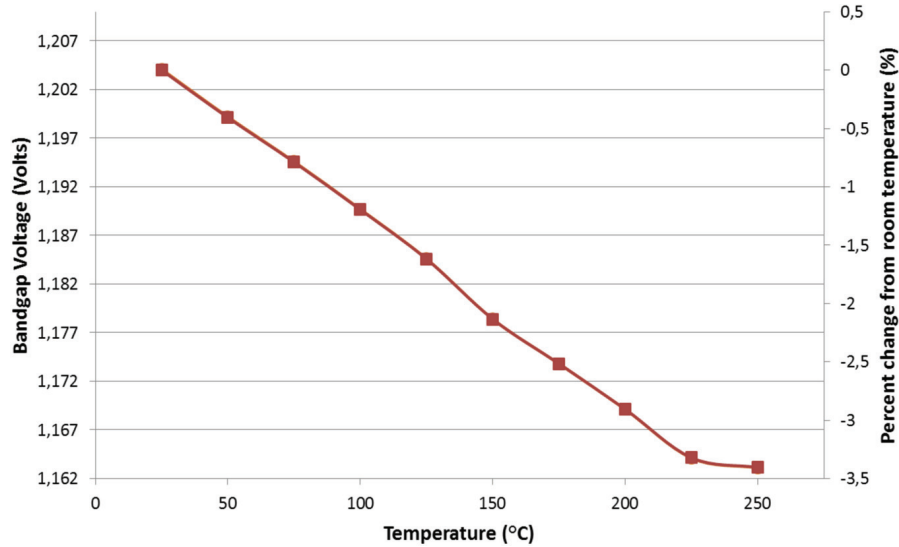
current-voltage mirror. The start-up circuit is also shown. In the case where there is no current flowing in either of the D1 or the D2 branches, Mp6 will provide the start-up current until the drain of Mp6 has increased high enough (one diode voltage drop) to stop the injection of startup current. The typical simulated performance of the bandgap voltage reference is presented in Table 4.5.

Table 4.5 Bandgap voltage generator simulation results

Parameter	SMCVM	Unit
Supply Voltage VDD	5	V
Output Voltage V_{ref}	1.27	V
Supply Current	134	μA
Temperature Range	-60 to 260	$^{\circ}C$
TC_{eff} at VDD = 3.3 V	24.4	ppm/ $^{\circ}C$
Line Regulation at 40 $^{\circ}C$	4.05	mV/V
Supply Sensitivity at 100 Hz	44	dB
Voltage Variation with temperature (per unit)	62.5	$\mu V/^{\circ}C$
$\frac{dV_{ref}}{dT}$		
Noise [1 Hz to 100 MHz]	85.8	μV_{rms}

4.3 Bandgap Voltage and Reference Current

The bandgap voltage was measured across temperature and the results are shown in Figure 4.7. At an analogue supply voltage of 5 V, the bandgap voltage has a temperature coefficient of 151 ppm/ $^{\circ}C$ between 25 $^{\circ}C$ and 250 $^{\circ}C$, with a nominal voltage of 1.2041 V. The bandgap voltage drops by 3.4% between 25 $^{\circ}C$ and 250 $^{\circ}C$.

**Figure 4.7** Bandgap voltage (actual and percent change) vs. temperature.

The reference current ($I_{reference}$) is generated by applying the bandgap voltage across an external 5.8 k Ω resistor with a low temperature-coefficient. At an analogue supply voltage of 5 V, the reference current has a temperature coefficient of 136 ppm/ $^{\circ}$ C between 25 $^{\circ}$ C and 250 $^{\circ}$ C, with a nominal value of 201.7 μ A. The reference current drops by 3.1% between 25 $^{\circ}$ C and 250 $^{\circ}$ C. Figure 4.8 demonstrates the layout of the bandgap voltage reference cell. The table in Figure 4.9 shows the nominal simulation results for the bandgap voltage reference cell including extracted post-layout parasitics.

4.4 Bias Network

Bias network generated reference voltage constant over temperature, reference current which is distributed across the chip and reference voltages for various analog cells of the ASIC. It consists of a bandgap voltage generator, a voltage-to-current converter, a voltage generator and current mirrors banks which replicate and distribute reference currents.

4.4.1 Top Level Schematic Diagram

The pin Vbg is connected to the bandgap output and routed to the pad to measure the bandgap voltage and overdrive it if necessary. Rport is a node for connecting an external resistor with low temperature coefficient for precise current generation. Iref_ovdrv pin is routed to the output pad. This is a backup pin which should be used to inject reference current in case of voltage-to-current converter failure. The rest pins are internal. IrefXX is denoting the reference bias currents with for OpAmps and comparators, while IexcXXX, IoXXX are denoting the high accuracy excitation and reference currents. vXXX is used for the reference voltages.

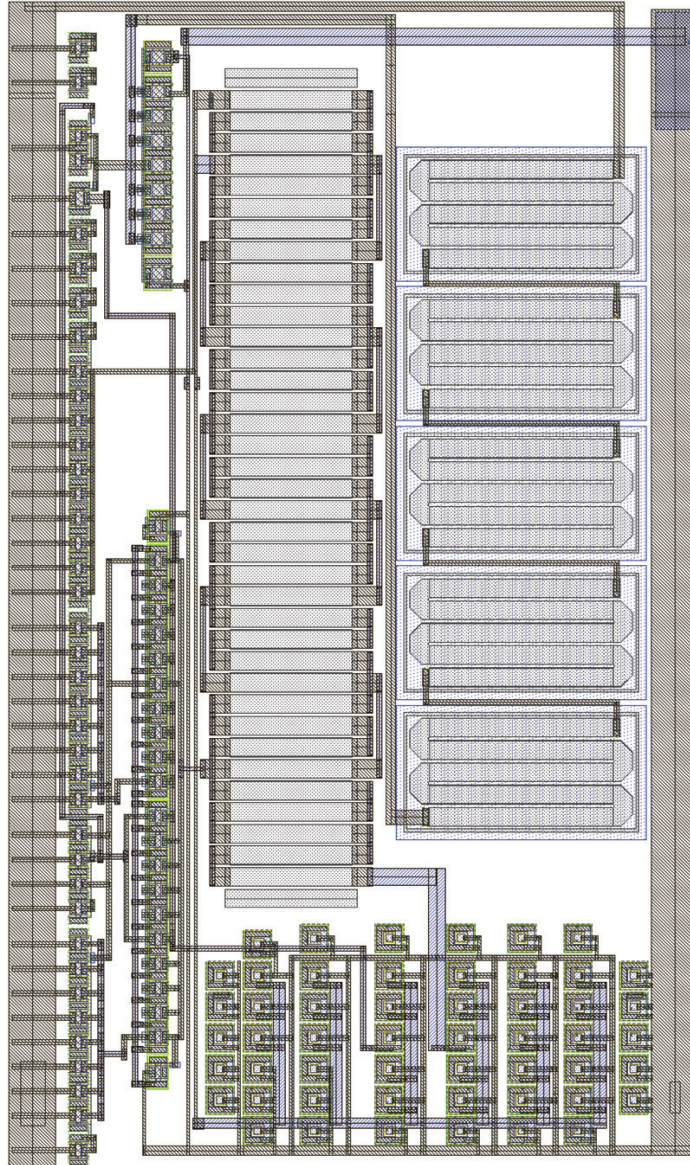


Figure 4.8 Layout of the bandgap voltage reference cell.

Parameter	SMCVM	Unit
Supply Voltage VDD	5	V
Output Voltage V_{ref}	1.27	V
Supply Current	134	μA
Temperature Range	-60 to 260	$^{\circ}C$
TC_{eff} at VDD=3.3V	24.4	ppm/ $^{\circ}C$
Line Regulation at 40 $^{\circ}C$	4.05	mV/V
Supply Sensitivity at 100 Hz	44	dB
Voltage Variation with temperature (per unit) $\frac{dV_{ref}}{dT}$	62.5	$\mu V/^{\circ}C$
Noise [1 Hz to 100 MHz]	85.8	μV_{rms}

Figure 4.9 Post-layout extraction simulation results of the bandgap voltage cell over PVT corners.

Table 4.6 Simulation results

Specification	Min	Nom	Max	Units	Note
Supply voltage		5		V	
Bias current	30	55	70	μA	
Current consumption			860	μA	
Temperature	-60		+225	$^{\circ}C$	
Input voltage	0.5		4.5	V	
Load current	-100		100	μA	
Capacitive load	0		3	pF	
Input capacitance			0.8	pF	at 10 Hz
DC open-loop gain	64		113	dB	
3-dB bandwidth in voltage follower configuration	2.6		23.3	MHz	
Phase margin	52		99	$^{\circ}$	
Gain margin	5.8		40	dB	
Integrated output noise in voltage follower configuration			0.15	mV	– Flicker noise is not included into simulation models – Ideal reference current source – Range: 10 Hz–1 GHz
Systematic offset voltage	-0.23		6	mV	Caused by output stage class AB biasing

4.4.2 Bias Network Layout

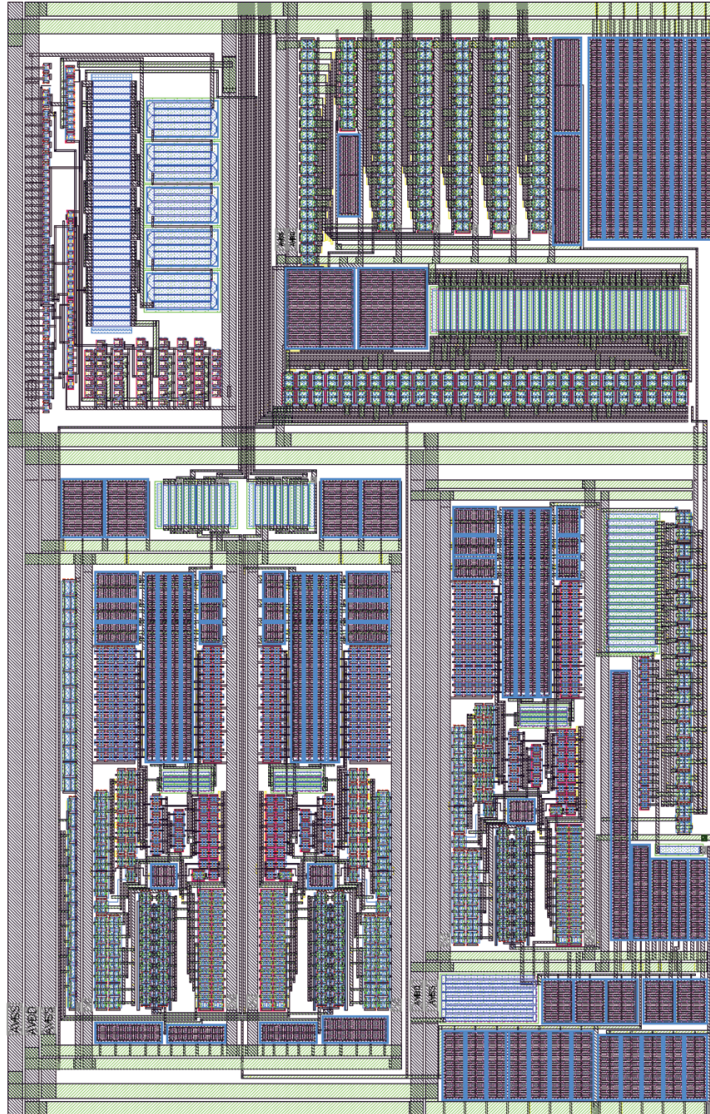


Figure 4.10 Bias network layout.

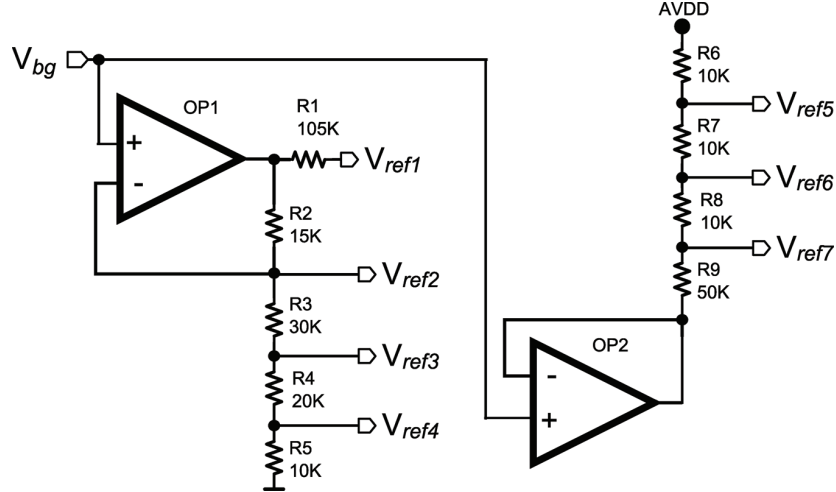


Figure 4.11 Reference voltages generator schematic diagram.

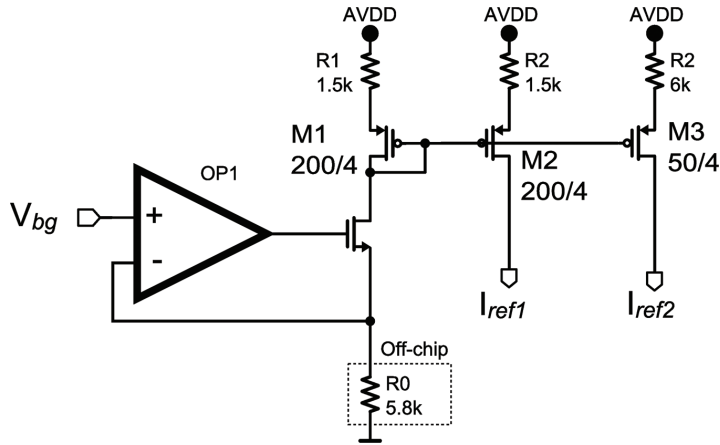


Figure 4.12 Schematic diagram of voltage to current converter.

4.4.3 Reference Voltages Generator

Reference voltage generator generates 6 different voltages from a bandgap output voltage. The values of the voltage values are: 3.6 V, 4.53 V, 4.06 V, 1.58 V, 634.9 mV and 211.6 mV. The simulation results of the voltage reference generator are presented in the Table 4.7.

Table 4.7 Simulation results of the voltage reference generator

Specification	Symbol	Value			Units	Notes
		Min	Nom	Max		
Temperature range		−50		250	°C	
Supply voltage			5		V	
Supply current		1.12	1.14	1.17	mA	
Output voltage	V _{3v6}	3.60145	3.601	3.60117	V	
Output voltage	V _{4v52}	4.53372	4.534	4.53382	V	
Output voltage	V _{4v05}	4.06745	4.067	4.06762	V	
Output voltage	V _{1v5}	1.5872	1.587	1.5876	V	
Output voltage	V _{0v6}	634.8834	634.9	635.050	mV	
Output voltage	V _{0v2}	211.6277	211.6	211.6514	mV	
RMS noise	V _{onRMS}	32.03	37.27	49.12	μV	Range: 1 Hz–1 GHz

4.4.4 Voltage to Current Converter

The voltage to current converter generated reference current using a stable bandgap voltage and a low TC external resistor. The nominal output current at Rport and Iref4x pin is 220 uA, which is defined as

$$I_{Rport} = \frac{V_{bg}}{R}$$

where Vbg = 1.27 V – bandgap voltage, and R = 5.8 kOhm – external resistor.

The feedback loop is sensitive to the capacitance at Rport. The phase margin of the open-loop circuit is lower the higher the parasitic cap at node Rport is. Figure 4.13 demonstrates the nominal simulations for small-signal stability of the open-loop voltage to current converter. To prevent ringing it is recommended to keep parasitic load capacitance at node Rport below 10 pF.

In the case of a voltage to current converter failure there is a possibility to define the reference current by an external current source. One of the possible failures of the voltage to current converter is the startup failure of the bandgap voltage reference. To disable the feedback loop pin Rport should be kept open or tied to AVDD via 1 MOhm external resistor. The external current is applied to the pin Iref_ovdrv. Another way to define the reference current externally is to apply the voltage at node Iref_ovdrv.

4.4.5 Current Mirrors

Current mirrors distribute generated reference currents across the ASIC. The cell consists of two mirror banks: the upper one with no source degeneration resistors for OpAmp and comparator bias currents (low precision current

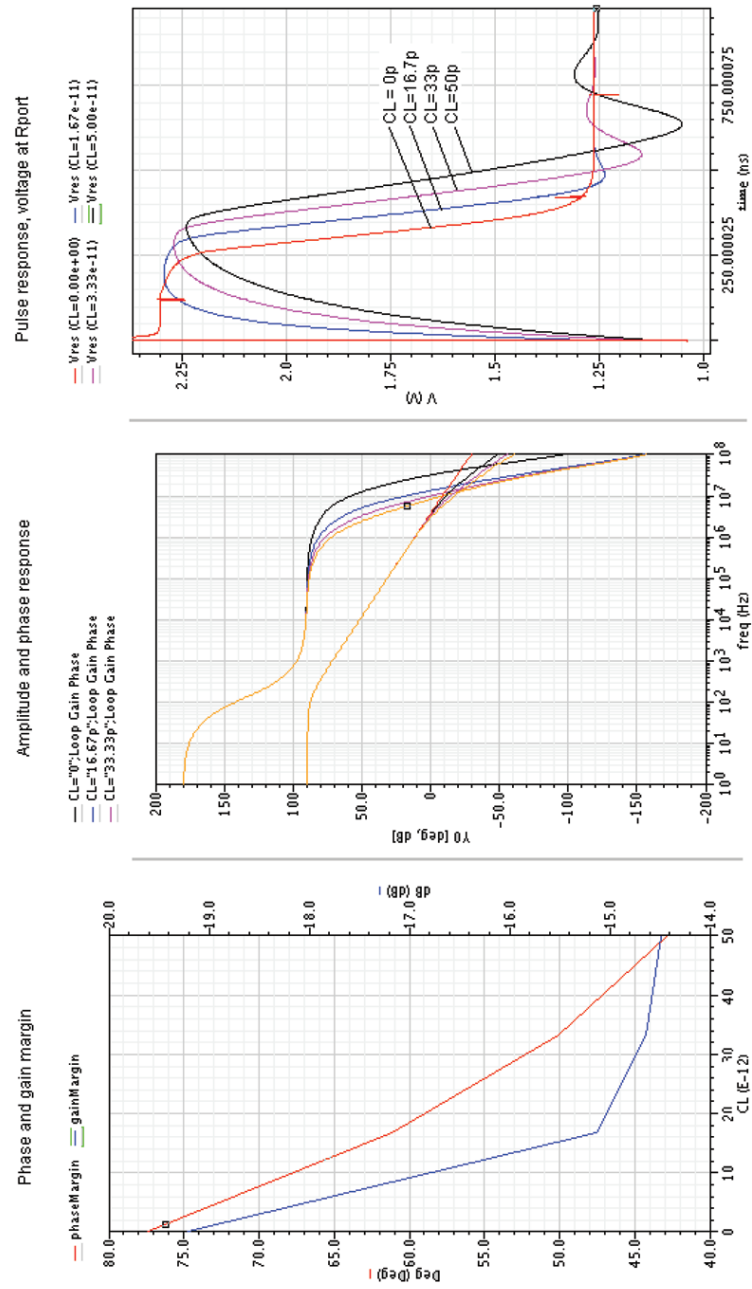


Figure 4.13 Nominal simulations for small-signal stability of the voltage to current converter.

mirror bank), and lower one with high accuracy current mirrors for excitation currents distribution and threshold current for QFreq channel.

4.5 Analog Multiplexer

The 11:1 analog multiplexer commutes 11 channels and test signals into one signal path as shown in Figure 4.14. The analog multiplexer consists of a series of transmission gates. Since transmission gates have some finite series resistance only capacitive loads can be driven by the analog multiplexer.

The multiplexer transient simulation results are shown in Figure 4.16. DC voltages applied to multiplexer inputs are $IN<0> \dots IN<10> = 0.2 \text{ V} \dots 4.2 \text{ V}$ with the step of 0.4 V . The output is loaded with 0.5 pF capacitance. The highest nominal series resistance of the multiplexer is $8.6 \text{ k}\Omega$ at room temperature.

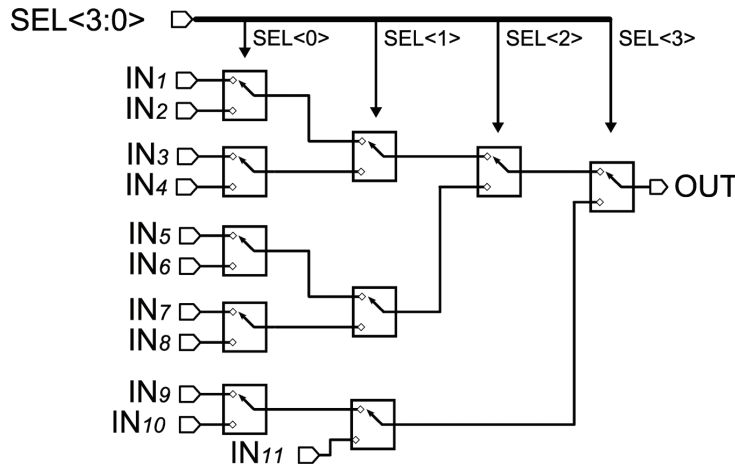


Figure 4.14 Analog multiplexer schematic diagram.

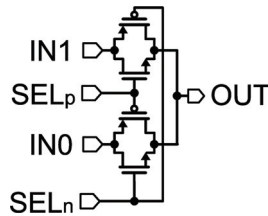


Figure 4.15 2:1 Multiplexer and transmission gate implementation.

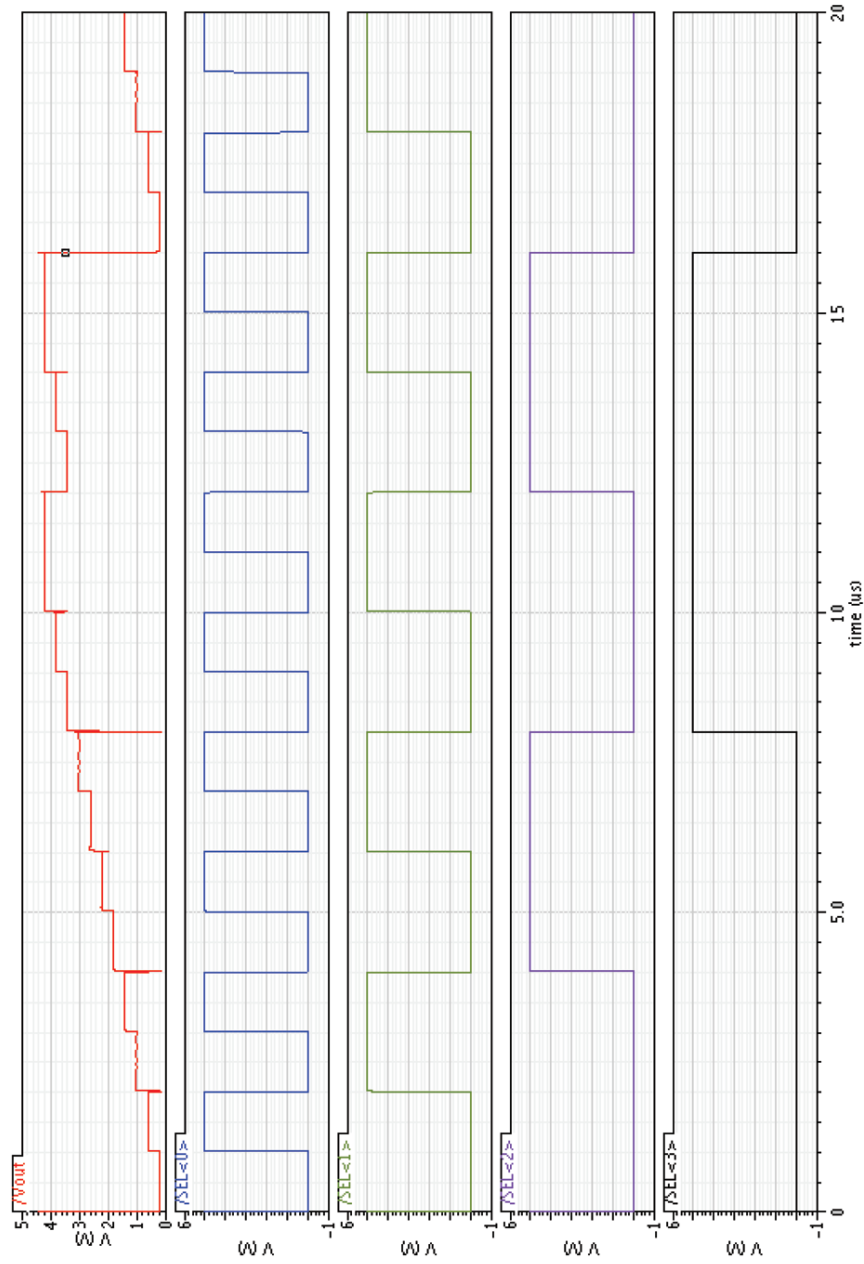


Figure 4.16 Multiplexer simulation results.

4.5.1 Layout of Analog Multiplexer

Layout of the multiplexer is demonstrated in Figure 4.17.

4.6 Single-Ended to Differential Converter

Since A/D converter used in this design has differential input single-ended to differential converter was designed to provide appropriate input for the ADC. Common mode voltage for converter is generated by the ADC and equals half of supply voltage.

4.6.1 Simulation Results

Figure 4.18 shows nominal simulation results for single-ended to differential converter. Simulation temperature is 27°C. Zero load capacitance was used in simulation testbench.

The output RMS noise is 190 uV in the band form 1 Hz to 1 GHz.

Output nodes of single-ended to differential converter are connected to output pads via 12 kOhm series resistors to prevent loading by high capacitive loads and stability degradation.

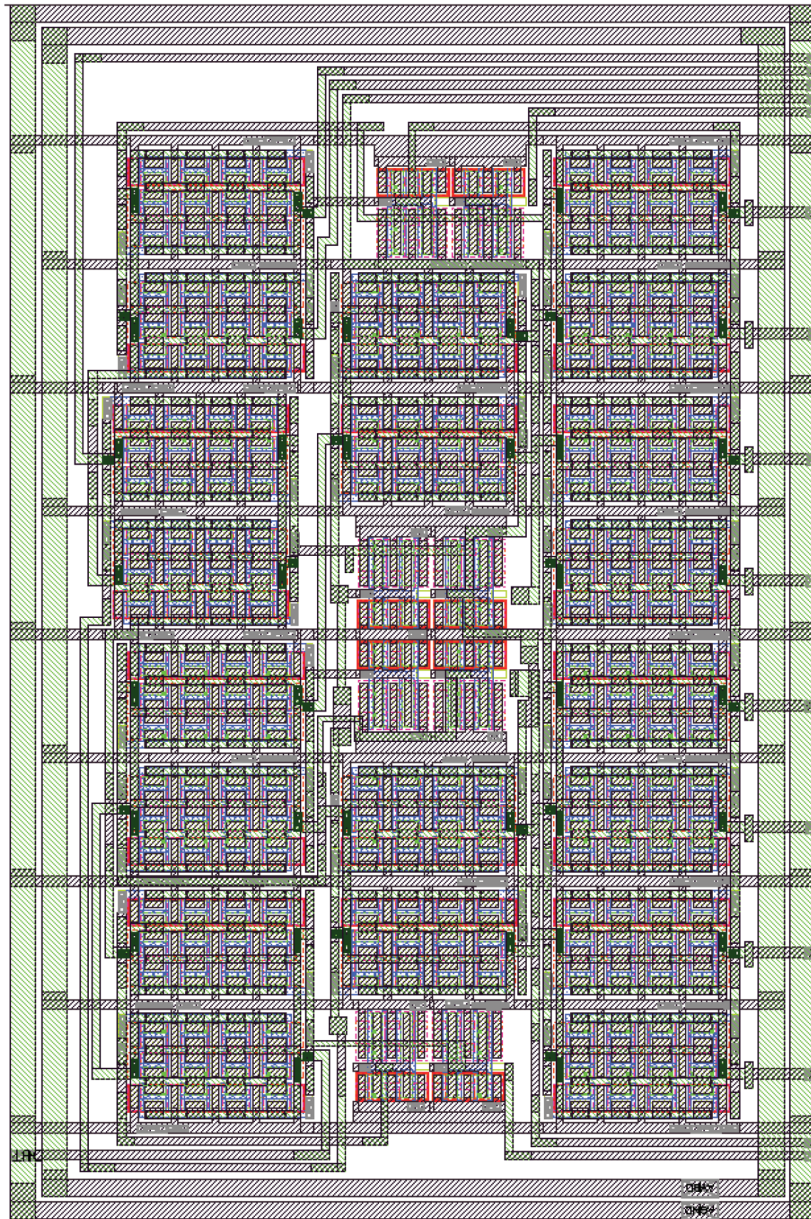


Figure 4.17 Layout of analog 11:1 multiplexer.

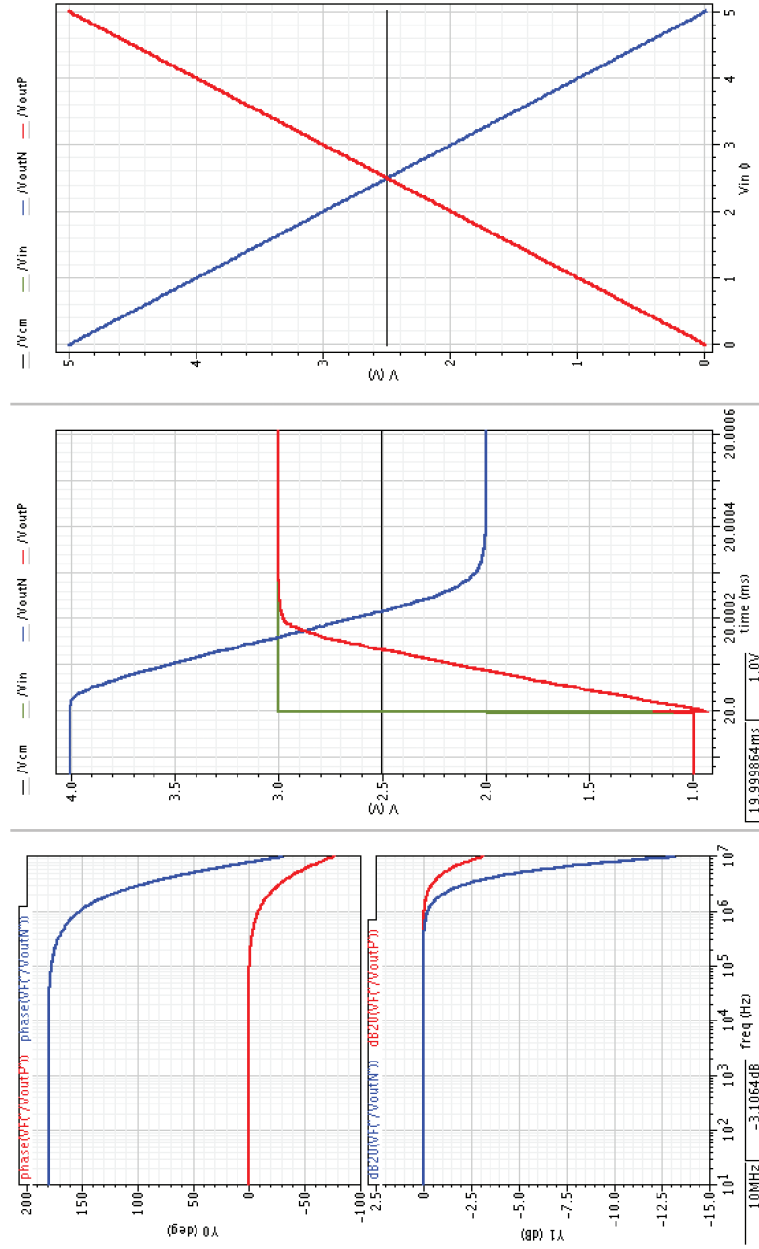


Figure 4.18 Nominal simulation results for single-ended to differential converter.

4.6.2 Layout of Single-Ended to Differential Converter

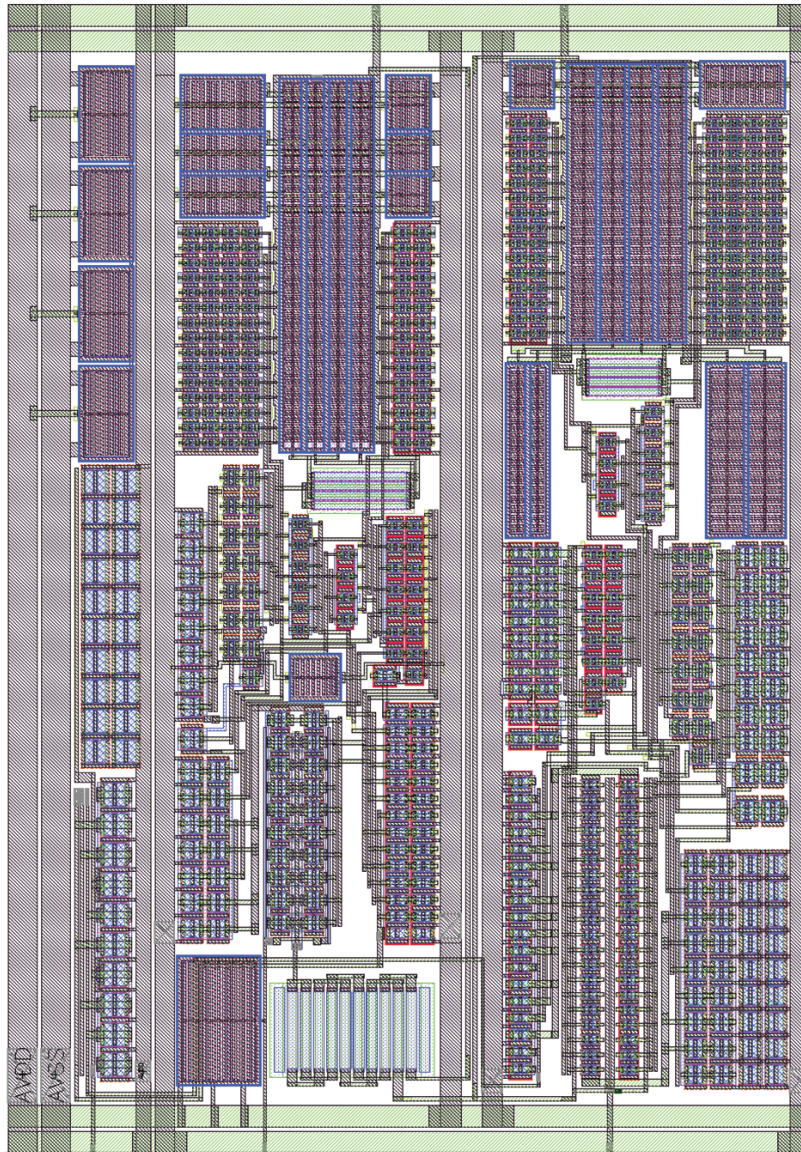


Figure 4.19 Single-ended to differential converter layout.

4.6.3 Single-Ended to Differential Converter

The SEDC is presented in Figure 4.20, where $OP1$ is a rail-to-rail opamp [3] and $OP2$ is the PMOS opamp presented in Section 4.1.2 [8]. The high resistivity $R1 - R10$ resistors have a value of $10\text{ k}\Omega$. The SEDC converts a high or low impedance, single-ended input signal to a low impedance, balanced, differential output suitable for driving the following ADC. The reference common mode voltage is set at the V_{cm} input. V_{outP} is directly provided by $OP1$, while V_{outN} is the 180° phase shifted version of the input generated by $OP2$ and the $R1 - R10$ resistors. On a single 5 V supply, the SEDC draws 1.2 mA, while the outputs can swing from 20 mV to 4.97 V. The SEDC can support SNR of 120 dB in a 1 kHz bandwidth and has a compact size of $750\text{ }\mu\text{m} \times 540\text{ }\mu\text{m}$.

4.6.4 Measurement Results

Figure 4.21 presents the micrograph of the designed instrumentation amplifier and single-ended to differential converter. Besides the HIGHTECS ASIC, the IA and the SEDC were fabricated on a test chip for electrical characterization over the $[25-225]^\circ\text{C}$ temperature range. The measured results of the temperature channel were presented in [1]. The measured DC gain of the IA used in the strain gauge signal conditioning channel is presented in Figure 4.22 and shows a difference of less than 1 dB over the $[25-275]^\circ\text{C}$ temperature range. Figure 4.23 shows the measured linearity of the PT100 based temperature channel at the input of the ADC at 225°C . The measured transfer function of the SEDC presented in Figure 4.24 shows a linear characteristic up to 225°C . A complete measurement system of the HIGHTECS ASIC, including the digital ARINC receiver was designed in VHDL and implemented on a Spartan 3E FPGA. The measured output waveform of the strain gauge channel via the

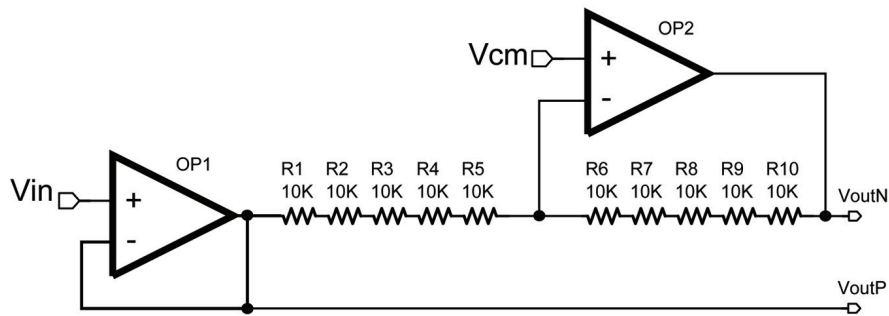


Figure 4.20 Schematic of the single-ended to differential converter.

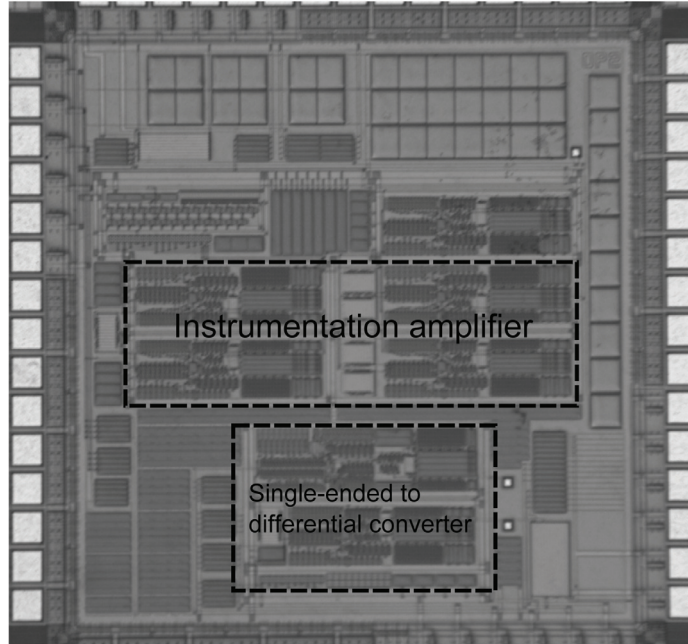


Figure 4.21 Micrograph of the designed instrumentation amplifier and single-ended to differential converter in X-FAB XI10 SOI process.

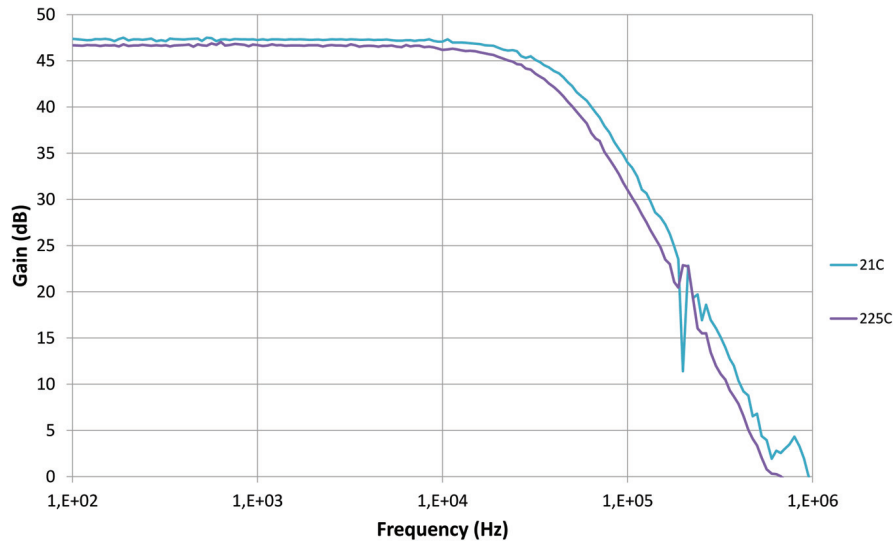


Figure 4.22 Measured DC gain of the instrumentation amplifier used in the strain gauge channel.

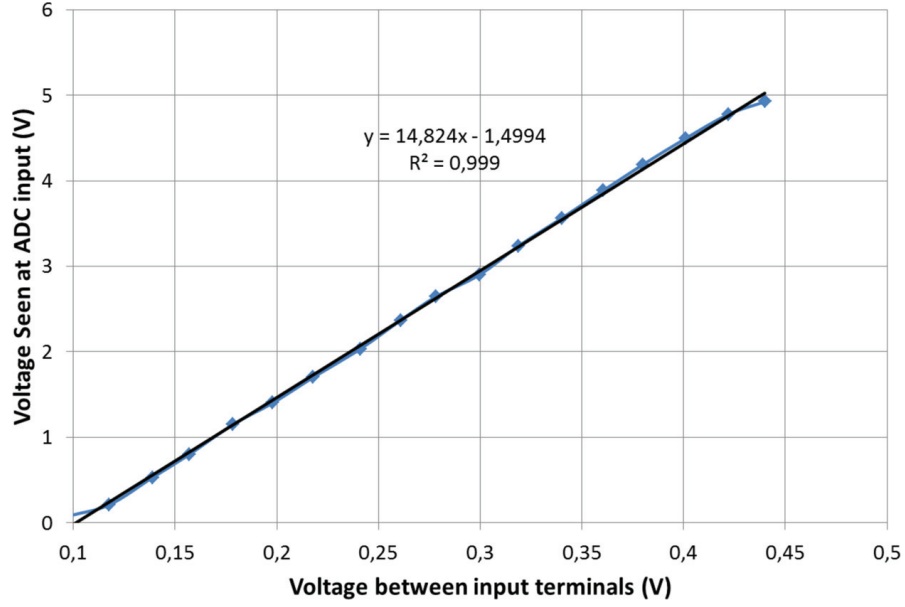


Figure 4.23 Measured linearity of the temperature channel at 225°C.

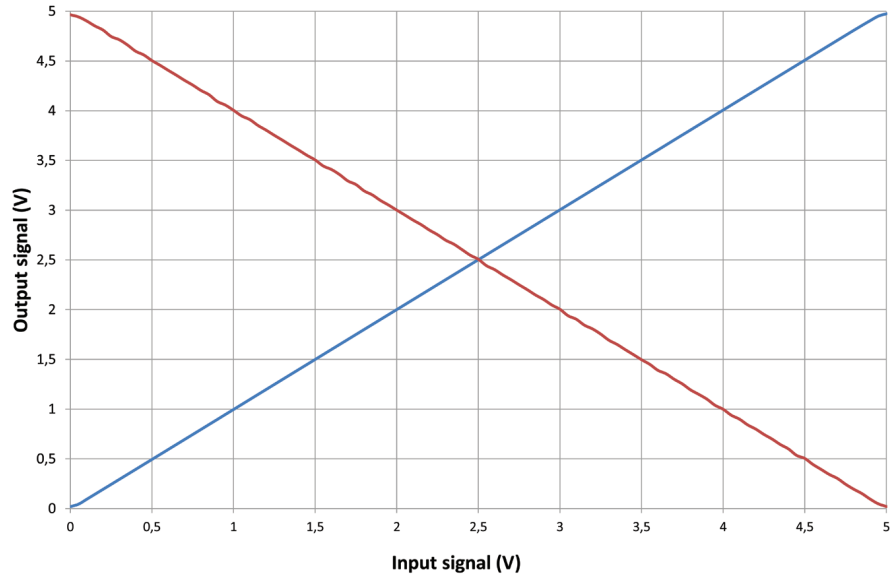


Figure 4.24 Measured transfer function of the single-ended to differential converter at 225°C.

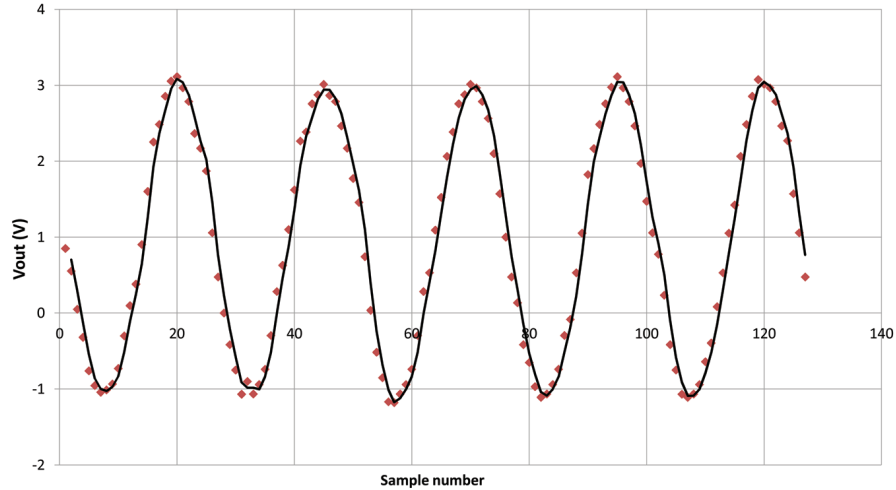


Figure 4.25 Measured output waveform of the strain gauge channel with a 16 mV sinusoidal input indicates a gain of 240.

Table 4.8 Specification versus achieved performance

Parameter	Specification	Measured	Units
T_{max}	200	225	°C
AVDD	5	5	V
IA DC Gain	47	46.8	dB
SEDC linearity range	[0.1–4.9]	[0.1–4.9]	V

IA, SEDC, ADC, ARINC transmitter and receiver is presented in Figure 4.25. This demonstrates the functionality of the complete signal conditioning chain from the input of the IA to the ARINC digital output. Table 4.8 presents the specification versus achieved performance. The IA and the SEDC are fulfilling their requirements at 200°C.

4.7 T1/TFo — Temperature Channels

4.7.1 Temperature Channels

The temperature channels T1, TFo1, and TFo2 are designed to excite a PT100 temperature-dependent resistor by applying a constant excitation current and conditioning the voltage signal coming off of the changing resistance. The block diagram for the sensor reading and signal conditioning is shown in Figure 4.26.

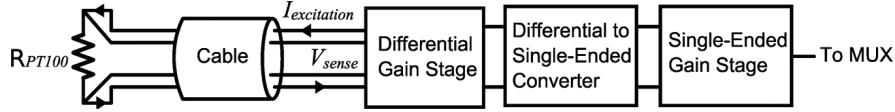


Figure 4.26 Temperature channel T1 signal conditioning diagram.

The excitation current is generated from a mirror of the reference current in the bias block. Ideally, this current does not vary over temperature, allowing the only signal variance to be the sensor resistance across temperature. The designed signal conditioning profile, where the blue area indicates the extreme voltages corresponding to a range of the excitation current ($I_{excitation}$) from 2.5 to 3 mA, and the green area shows the nominal profile corresponding to an excitation current of 2.7 mA.

The temperature sensor for these channels can be placed in the same or in a different temperature environment from the ASIC, as the excitation current will be minimally impacted by the temperature seen by the sensor. This channel also has been designed to determine and report open and short circuit fault conditions to the processing computer.

The excitation current measured in the previous section was applied across a PT100 RTD (Resistance Temperature Detector) at the TFo2 terminals. The measurement results are presented in Figure 4.27. The sensor was kept in the

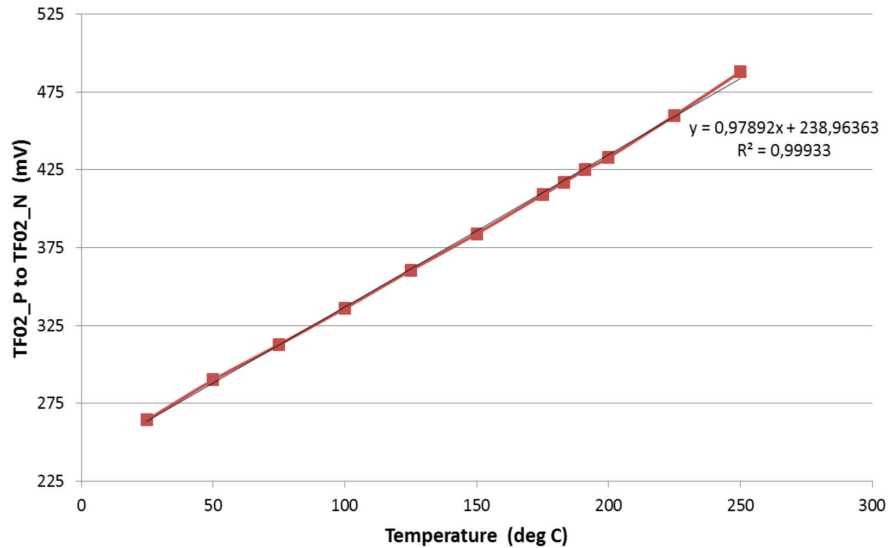


Figure 4.27 Voltage measured across TFo2 terminals vs. temperature.

same temperature environment as the ASIC and the resulting voltages were measured across temperature.

The RTD sensor is designed to be linear across temperature, and with an excitation current that has a low temperature dependence, the resultant voltage is highly linear across temperature. The data from a 5 volt analogue supply shows greater than 0.1% linearity ($R^2 = 0.99933$) between 25°C and 250°C.

PT100 is used as a sensor for T1 channel.

Sensor transfer function:

$$R_{PT100} = 99.4 + 0.379 \cdot T$$

Sensor gain:

$$k_{PT100} = 0.379 \frac{\Omega}{^{\circ}C}$$

For the specified temperature range

$$R_{PT100.min} = R_{PT100}(-60^{\circ}C) = 77.66\Omega$$

$$R_{PT100.max} = R_{PT100}(-130^{\circ}C) = 148.67\Omega$$

Taking sensor tolerances into account:

$$R_{PT100.min} \geq 75\Omega$$

$$R_{PT100.min} \geq 150\Omega$$

4.7.2 T1/TFo Operating Principle

Channel T1 comprises an instrumentation amplifier and an excitation current source which provides current for PT100 resistor. The voltage drop at PT100 is sensed by the instrumentation amplifier. Channel T1 uses four-terminal impedance sensing input.

Channel TFo is based on T1. The only difference is that TFo uses only two terminals for applying excitation current and sensing the voltage.

4.7.3 T1/TFo Functionality

4.7.3.1 Voltage-gain profile

The channel front-end incorporates three gain stages. The voltage-gain profile is shown in Figure 4.28.

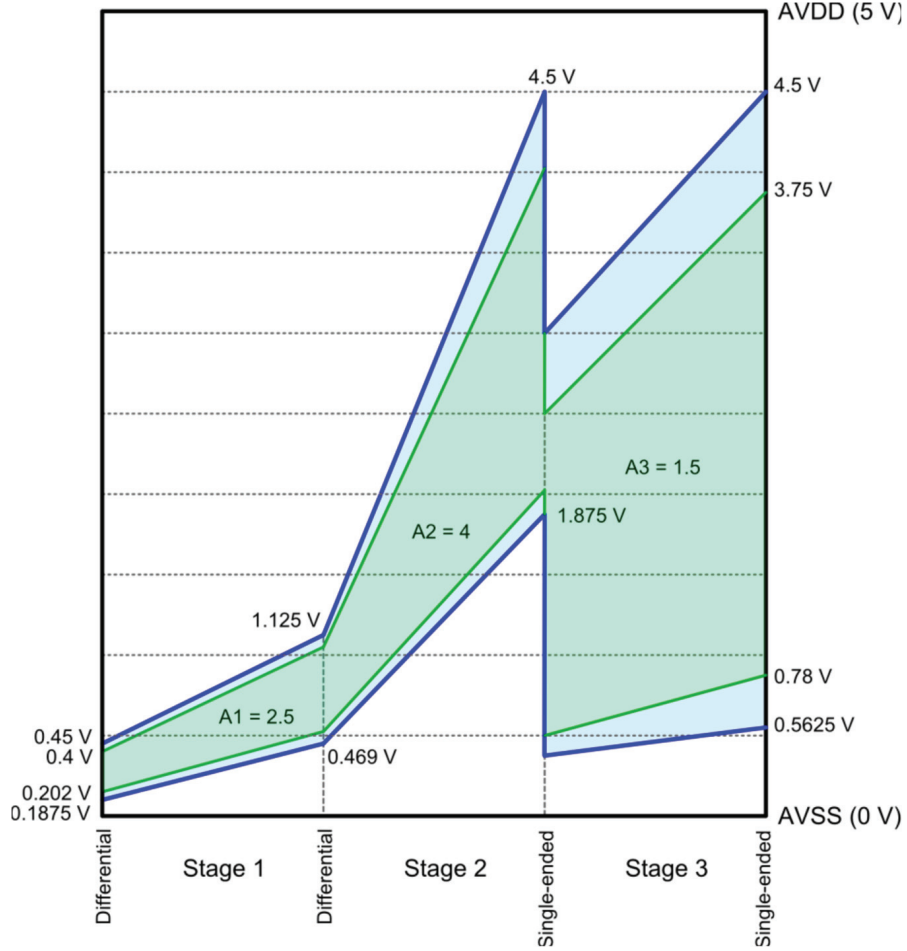


Figure 4.28 Voltage gain profile of the analog front-end. Blue area – extreme voltages, corresponding to 2.5 mA/3 mA excitation current. Green area – nominal profile, corresponding to 2.7 mA excitation current.

4.7.3.2 Static accuracy

$$\Delta T_{stat} = \frac{\Delta R_{stat}}{k_{PT100}}$$

where ΔT_{stat} is an equivalent resistance measurement error, defined as

$$\Delta R_{stat} = \Delta R_{IA} + \Delta R_{exc.temp} + \Delta R_{noise}$$

where ΔR_{IA} – resistance measurement error caused by an instrumentation amplifier,

$\Delta R_{exc.temp}$ – resistance measurement error caused by excitation current variation over temperature,

ΔR_{noise} – resistance measurement error caused by noise.

$$\Delta R_{IA} = \left(\frac{V_{out.meas} - V_{out.ideal}}{A_0} \right) / I_{exc.min}$$

where $V_{out.meas}$ – measured voltage at the output of instrumentation amplifier,
 $V_{out.ideal}$ – voltage at the output of an ideal instrumentation amplifier (no nonlinear distortions).

$$\Delta R_{exc.temp} = \frac{R_{PT100.max} \cdot \Delta I_{exc.temp.max}}{I_{exc.min}},$$

Finally,

$$\Delta R_{noise} = \Delta T_{noise} \cdot k_{PT100} = \frac{V_{out.noise.max}}{A_0 \cdot I_{exc.min}}$$

4.7.3.2.1 Static accuracy simulation for variable chip temperature and constant sensor temperature

The sensor temperature is kept at 130°C, which is the maximum specified temperature. Model sections for simulation are changed simultaneously for all elements (all-wp, all-tm etc.). The static error is calculated using the output voltage deviation from a constant value over temperature, gain of the IA and the gain of the sensor:

$$\Delta T = \frac{\Delta V_{out}}{A_0 \cdot I_{exc.min} \cdot k_{PT100}} = \frac{\Delta V_{out}}{15 \cdot 2.5 \text{ mA} \cdot 0.379 \frac{\Omega}{^\circ\text{C}}}$$

The accuracy is simulated with transistor-level bandgap and excitation current source and ideal 1.2 V reference and ideal excitation current source. Results shown here do not take into account instantaneous temperature error caused by the noise of instrumentation amplifiers. Simulation results of T1's output voltage over a variety of corner variation is presented in Figure 4.29. Transistor-level circuits for the bandgap voltage reference and excitation current source were used. The largest static error over three simulated cases is 4.5°C ($\pm 2.26^\circ\text{C}$) at $-60 \dots +250^\circ\text{C}$ temperature span, and 1.41°C ($\pm 0.7^\circ\text{C}$) at $+50 \dots +150^\circ\text{C}$.

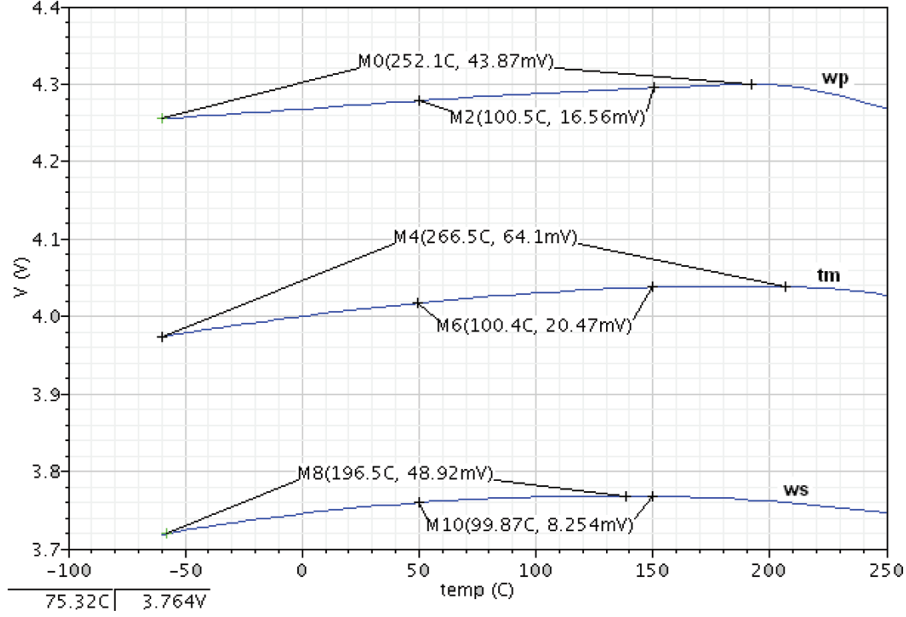


Figure 4.29 Output voltage of T1 channel. Transistor-level bandgap and excitation current source. The largest static error over three simulated cases is 4.5°C ($\pm 2.26^{\circ}\text{C}$) at $-60 \dots +250^{\circ}\text{C}$ temperature span, and 1.41°C ($\pm 0.7^{\circ}\text{C}$) at $+50 \dots +150^{\circ}\text{C}$.

4.7.3.2.2 Static accuracy simulation for variable chip temperature and variable sensor temperature

The temperature range for this simulation is $-60^{\circ}\text{C} \dots +130^{\circ}\text{C}$, as specified in specs. The chip temperature follows the sensor temperature.

4.7.3.3 Temperature error due to quantization error

Assuming 12-bit ADC and 4 V input voltage range, temperature error caused by quantization error is:

$$\Delta T_q = \frac{\Delta R_q}{k_{PT100}} = \frac{\Delta V_{out.q}}{A_0 \cdot k_{PT100} \cdot I_{exc.min}} = \frac{4/2^{12}V}{15 \cdot 0.379 \frac{\Omega}{^{\circ}\text{C}} \cdot 2.5 \text{ mA}} = 0.07^{\circ}\text{C}$$

4.7.3.4 Input ESD protection

Voltage levels at chip inputs are kept below 5 V at normal operating conditions. A pad cell used for T1/TFo inputs is “APRBDF”. The schematic of the ESD protection circuitry is shown in Figure 4.32.

4.7.3.5 Short and open circuit detection

The following short/open conditions are detected:

- Short at pins MP and MN;
- Open at pins MP and MN;
- Open at pins EP and MP, EN and MN (channel T1 only)

The following short/open conditions are not detected:

- Short at pins EP and MP, EN and MN (channel T1 only)

4.7.4 Mirrored Bias Current for Temperature Probe Excitation

Three of the temperature channels have been designed to work with temperature-dependent resistors like the PT100. To be able to measure the resistance, and thus compute the temperature seen by the sensor, an excitation current is provided via a multiplying mirror of the reference current.

Excitation current mirror contains source degenerating resistors to increase output impedance of the current sources and reduce current dependence on temperature. Simulation results of T1's output voltage over a variety of corner variation is presented in Figure 4.30. Ideal excitation current source

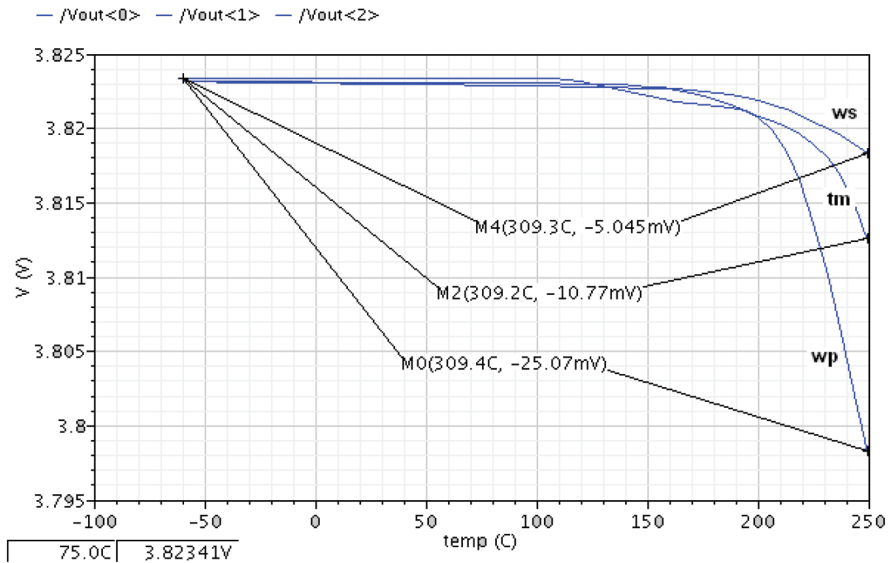


Figure 4.30 Output voltage of T1 channel. Ideal excitation current source and reference voltage source. The largest static error over three simulated cases is 1.76°C ($\pm 0.88^\circ\text{C}$) at -60 ... +250°C.

and reference voltage source were used. The largest static error over three simulated cases is 1.76°C ($\pm 0.88^{\circ}\text{C}$) at $-60 \dots +250^{\circ}\text{C}$.

The simulated resistance error over corner variation is presented in Figure 4.31. Transistor-level circuits for the bandgap voltage reference and excitation current source were used. The largest static error over three simulated cases is 0.67 Ohm, which corresponds to 1.77°C ($\pm 0.89^{\circ}\text{C}$) at $-60 \dots +130^{\circ}\text{C}$.

4.7.5 T1/TFo Channels Schematic Diagrams

4.7.5.1 T1 top level connection

No off-chip discrete components for T1/TFo are required.

The top level schematic of T1 channel is presented in Figure 4.33.

Channel TFo2 was measured across temperature and the results are shown in Figure 4.34. The excitation current is given by the solid line and the mirroring ratio between the excitation current and the reference current is given by the dotted line.

The excitation current has a temperature coefficient of 169 ppm/ $^{\circ}\text{C}$ between 25°C and 250°C , with a nominal value of 2.43 mA at room temperature. The mirroring ratio has a temperature coefficient of 326 ppm/ $^{\circ}\text{C}$ between 25°C and 250°C , with a nominal designed ratio of 12.5. These low temperature coefficients are indicative of the stability of the biasing block across temperature.

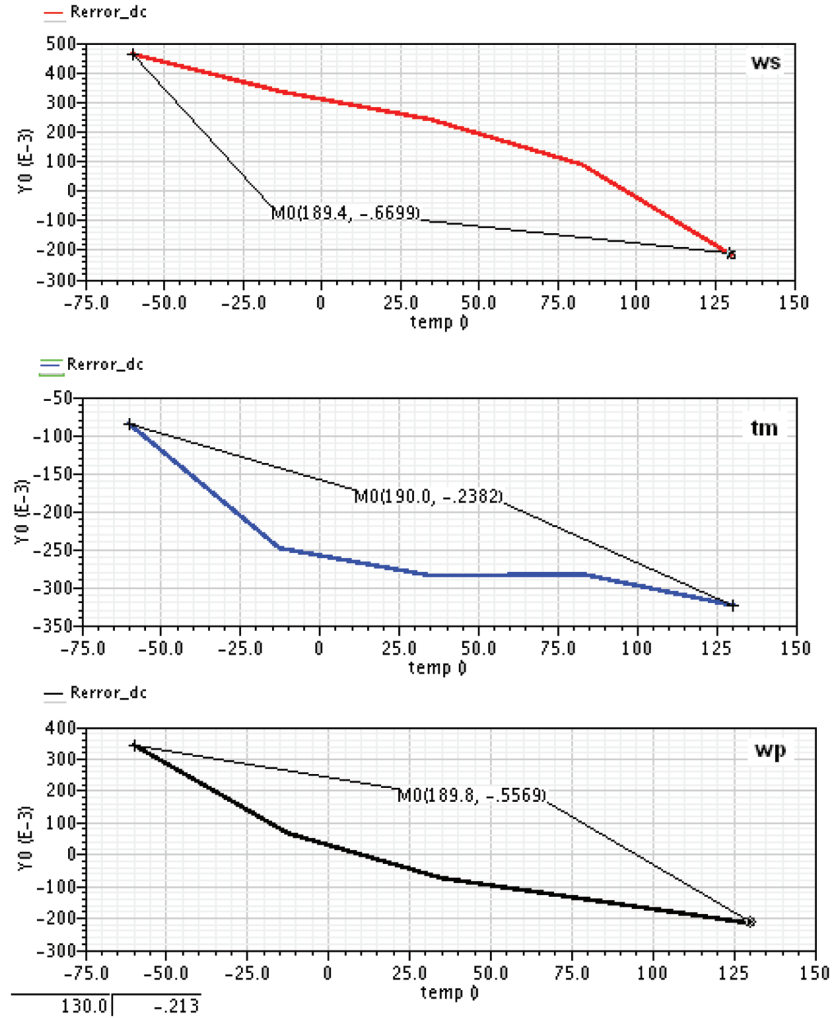


Figure 4.31 Simulated resistance error. Transistor-level bandgap and excitation current source. The largest static error over three simulated cases is 0.67 Ohm, which corresponds to 1.77°C ($\pm 0.89^\circ\text{C}$) at $-60 \dots +130^\circ\text{C}$.

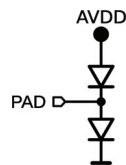


Figure 4.32 Input pad for channel T1/TFo (“APRBDF”).

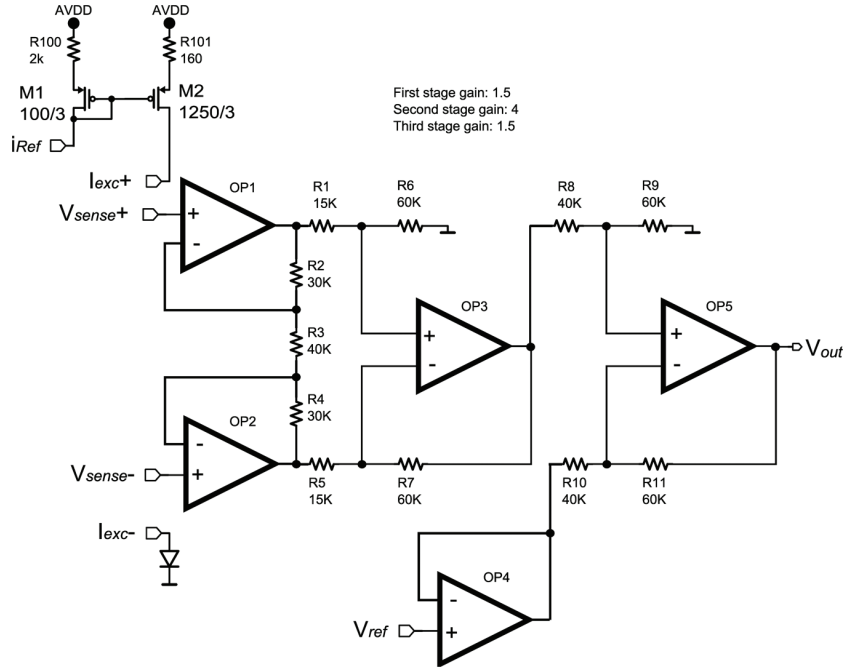


Figure 4.33 T1 top level schematic.

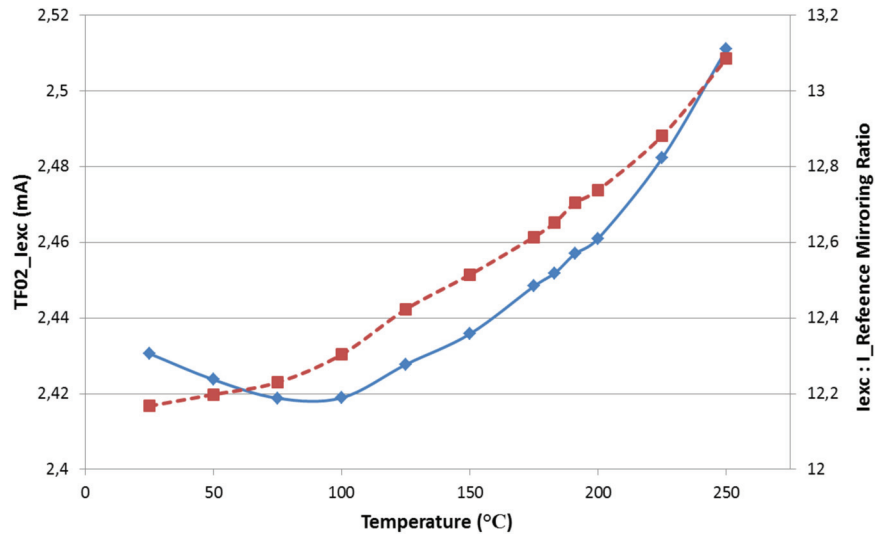


Figure 4.34 TF02 $I_{excitation}$ (solid) and mirroring ratio (dotted) vs. temperature.

4.7.6 T1/TFo Channels Layout

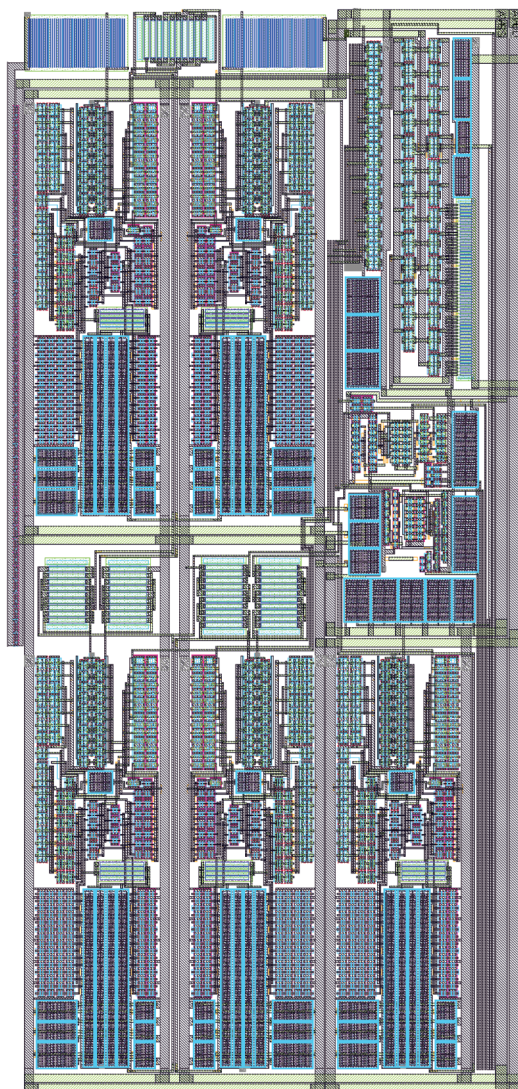


Figure 4.35 T1/TFo layout – size: 730 μm $\times$ 1530 μm .

4.8 SG2 — Strain Gauge Channel

In this section the error budget of the PT100 based temperature channel and the IA for the strain gauge channel are presented. The performance of the IA used in the temperature channel was previously presented in [1]. The block diagram for the strain gauge signal conditioning IA is shown in Figure 4.36, where *OP1*, *OP2* and *OP3* are PMOS input opamps. The IA is connected to a strain gauge bridge and has to perform a signal amplification of 240 (47 dB) based on the sensor's measurement range specification. In addition to signal amplification, the conditioning channel has to detect the *OPEN* or *SHORT* to 10 V conditions of the input terminals. The IA draws 3 mA from a 5 V supply and has a size of $1290\ \mu\text{m} \times 725\ \mu\text{m}$. The voltage at V_{ref} is provided by the voltage reference block presented in [1].

4.8.1 Testing of HIGHTECS Module

The HIGHTECS module was assembled as shown in Figure 4.37, the module consisted of the HIGHTECS hybrid circuit was selected to be built into a module to be tested, and the high temperature printed circuit board with resistors wired to the connectors within the stainless steel module.

The output from SG2 sensor was selected for testing over the range of voltage MN9.2 to 9.8 V with MP set at 9.5 V in steps of 0.05 V from -40°C to $+225^\circ\text{C}$.

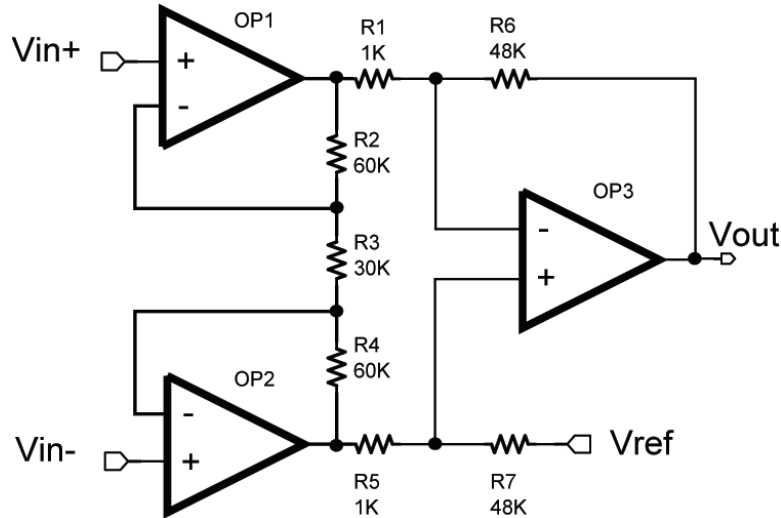


Figure 4.36 Simplified schematic of the strain gauge signal conditioning channel.

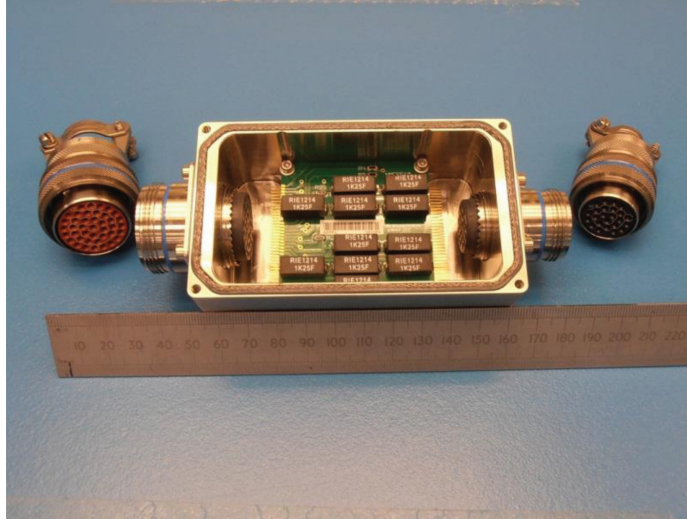


Figure 4.37 HIGHTECS module.

The results show a predominantly linear output at temperatures of 20°C and above, when the outputs with error codings are removed from the analysis.

4.9 QFREQ — Frequency Channel

4.9.1 Introduction

In this section, we focus on the mixed signal conditioning and digital counting units to calculate the frequency of a signal coming from an electromagnetic sensor facing a phonic wheel of an aeroengine [3, 9]. The phonic wheel consists of two intermeshed teeth on the loaded engine drive shaft and another set of teeth on the unloaded shaft end in the same plane. The produced signal enables to measure the frequency and the phase between the loaded and unloaded phonic wheel enables to calculate the torque. The sensor signal can have amplitudes up to 70 V_{pp} with sharp edges and a maximum frequency of 4 kHz.

A novel CMOS SOI current peak detector was developed to detect and process the input signal [3]. Current peak detectors have been previously published in [10–13]. In [10, 12], the disadvantage of the peak detectors is that the hold capacitor is charged by the input current. In Figure 4.38 [11], for a high sensitivity of the peak detector, the output resistance of the feedback transistor PI and the input current source I_{hr} must be high, while for a high

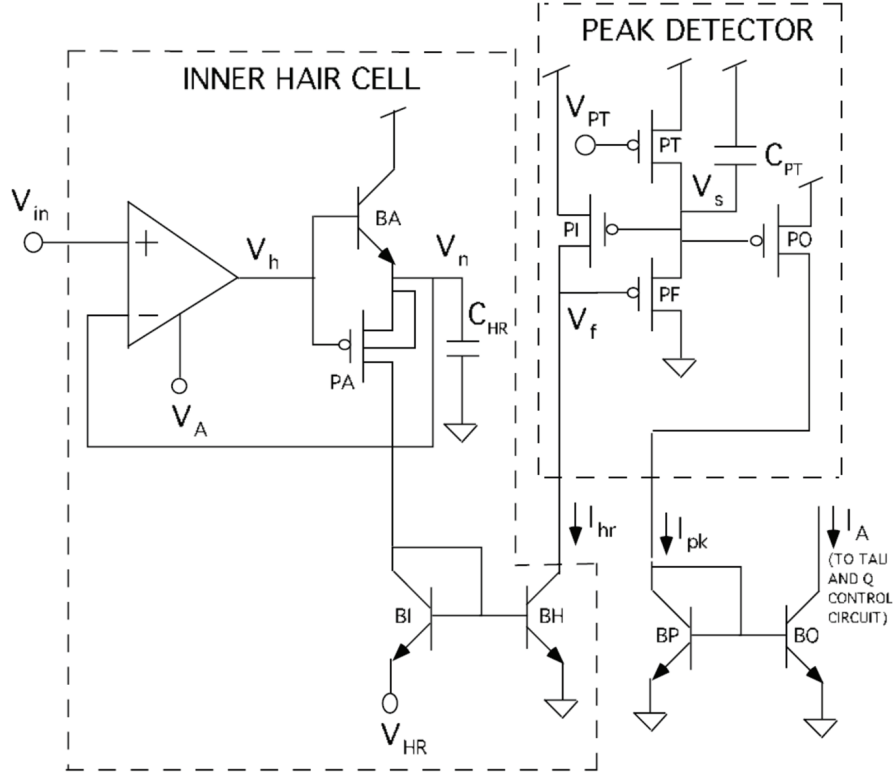


Figure 4.38 Peak detector presented in Figure 9 of [11]. (c) Springer. Reprinted with permission.

charging speed, the output impedance of the PI transistor and I_{hr} must be low to provide good driving strength for the PF transistor. In [13], Figure 4.39, the peak detector is a trade off between the sensitivity and speed, as follows: for a high sensitivity the output of M_2 , M_3 and I_a must be high, while for a high charging speed, the output resistance of M_3 and I_a must be low to provide good driving strength for M_5 .

The section is organized as follows. Section 4.9.2 describes the system architecture, the input signal definition and derives the unit specifications. Section 4.9.3 presents the operation principle and the design methodology of the proposed detector. The proposed CMOS SOI current peak detector is presented in Subsection 4.9.3.2. Its main advantages over previously published architectures are stable operation over a wide temperature range and high

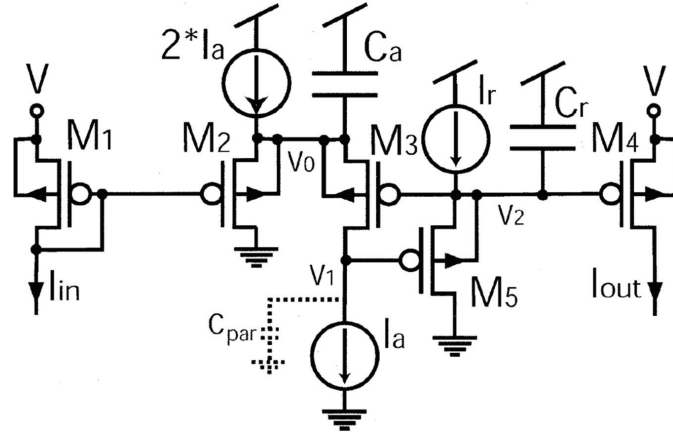


Figure 4.39 Peak detector presented in Figure 2 of [13] (c) IEEE. Reprinted with permission.

speed due to low charging time of the external capacitor. The proposed pulse selector is presented in Subsection 4.9.3.4. Their main advantages are that they are internally generating and processing digital pulses, therefore eliminating the need of an analog-to-digital converter (ADC) in the signal path. Experimental results and conclusions are presented in Sections 4.9.4.

4.9.2 System Architecture

The HIGHTECS ASIC is made up of several system level blocks shown in Table 4.9 and connected as in Figure 4.40.

Functionally, the reference voltage generator and bias circuits provide the needed voltages and currents for the opamp-based signal conditioning circuits for each type of sensor. The signal flow then goes from the excitation of the

Table 4.9 Functional blocks included in the ASIC

List of Functional Blocks	
Bandgap Reference Generator	4 Temperature Channels
Reference Current Generator	4 Strain Gauge Channels
Bias Voltages Generator	3 Pressure Sensor Channels
Global Current Mirrors	ADC
Digital Input	ARINC 429 Driver
Frequency Signal Conditioning	ARINC 429 Control Sequencer
Frequency Pulse Counting Logic	

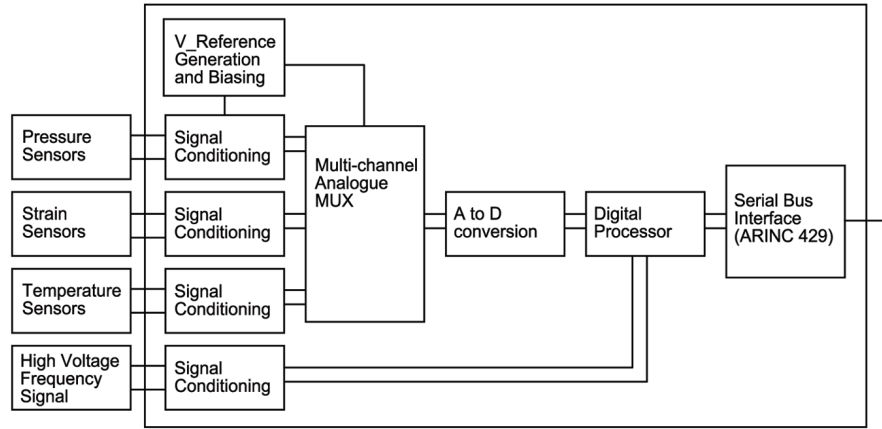


Figure 4.40 HIGHTECS ASIC function level block diagram including the signal conditioning processing the high voltage frequency signal.

sensor, to the signal conditioning, to the multi-channel analogue multiplexer (MUX) and the ADC, and then to the ARINC429 [14] databus and out to the processing computer. The serial bus interface (ARINC 429) facilitates the data transmission from the ASIC to the FADEC or EHMS. With the exception of the ADC, all of the other HIGHTECS ASIC blocks have been customly designed during the project. The signal conditioning unit processing the high voltage frequency signal was integrated onto the HIGHTECS ASIC [1, 3], and requires only two pairs of external resistors and capacitors for signal conditioning and six external resistors for ESD protection. The block diagram of the frequency signal conditioning unit is presented in Figure 4.41. The input stage includes the input diodes, the current mirrors and the ESD protection. The current path (I_{path}) includes the current peak detector, the current divider and the current comparator. The voltage path (V_{path}) includes the voltage-peak detector, the voltage divider and the voltage comparator. The input diodes perform the voltage-to-voltage or voltage-to-current conversions. The current mirrors are copying the current to the following stages in the current and voltage path. The ESD pads ensure that the voltage at the input of the ASIC does not exceed 5 V during normal operating conditions. The current peak detector includes a current comparator, an opamp-based voltage peak detector and a current source. The pulse selector is generating a digital output signal highly immune to harsh environment conditions. The frequency pulse counting logic is embedded into the digital processor following the HIGHTECS ADC.

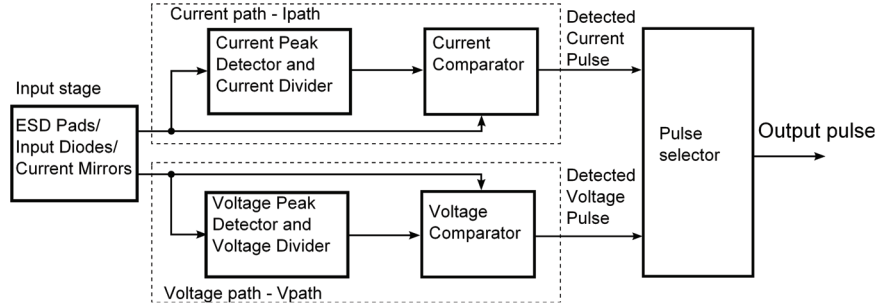


Figure 4.41 Block diagram of the frequency signal conditioning unit for rotating equipment.

The circuit implementation of the frequency signal conditioning unit is presented in Section 4.9.3.

4.9.2.1 Input signal definition

The definition of a typical input signal is presented in Figure 4.42, where A is the signal amplitude, T is the signal period, N_{max} is the maximum noise voltage, V_t is the threshold voltage, ΔV_t is the target hysteresis window opening, A is the average signal peak level, and ΔA_i is the instantaneous signal peak level deviation. The parameters of the rotational system are defined as $F_{min} = 50$ Hz and $F_{max} = 4$ kHz. The frequency signal conditioning unit has to provide the information about the instantaneous period T and cyclic ratio $C = t/t'$ of the input signal based on the pulses detected in the current and voltage paths discussed above. The instantaneous period and cyclic ratio are calculated by a digital counter running on a reference clock and triggered by

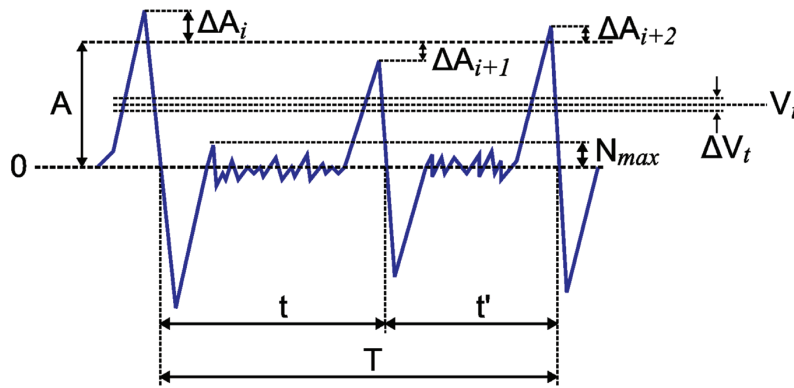


Figure 4.42 Input signal model.

the detected pulses. The reference frequency value is determined based on the cyclic ratio C measurement accuracy requirements. Since C is calculated digitally, t and t' must be measured precisely enough to fulfill the requirements for ΔC .

4.9.2.2 Theoretical performance

To achieve the accuracy of $\Delta C = 0.0001$, $1/\Delta C = 10000$ periods of the reference signal must fit into the shortest period of the input signal, as shown in the equation:

$$F_{ref} \geq F_{max} \cdot \frac{1}{\Delta C} = 4000 \text{ Hz} \cdot 10000 = 40 \text{ MHz} \quad (4.2)$$

Given the reference frequency, the accuracy of the frequency measurement is:

$$\Delta F = \frac{F_{max}}{F_{ref}} \cdot 1 \text{ Hz} = 0.0001 \text{ Hz}, \quad (4.3)$$

where as implied by 1 Hz constant, the precondition is that both the count of F_{ref} and the count of input pulses are integrated for at least 1 s. The same frequency and cyclic ratio accuracy can be achieved with lower clock frequency by averaging the counts over several signal periods. Among the advantages of lower clock frequency is more reliable operation of digital counter and arithmetic unit over wide temperature ranges, larger choice of clock generators (for example, quartz oscillators) etc. We have chosen as specification a value of $F_{ref} = 10 \text{ MHz}$ for the clock frequency. The minimum counter resolution is defined by F_{min} and F_{ref} , as follows:

$$n_c \geq \log_2\left(\frac{F_{ref}}{F_{min}}\right) = \log_2\left(\frac{40 \text{ MHz}}{50 \text{ Hz}}\right) = 19.6096 \text{ bits} \quad (4.4)$$

A counter with a resolution of 20 bit was implemented.

The threshold voltage should lie in between the maximum noise voltage and minimum positive signal peak level in order to minimize the risk of miscounts:

$$V_t = \frac{(A - \max\{\Delta A_i\}) - N_{max}}{2} + N_{max} \quad (4.5)$$

Hysteresis opening ΔV is 10% of the voltage range free of noise and amplitude variations.

$$\Delta V_t = \frac{A(1 - \frac{\Delta A\%}{100\%}) - A\frac{N\%}{100\%}}{10} \quad (4.6)$$

We define the instantaneous frequency error as follows:

$$\Delta F_i = F_{sig,i} - \frac{F_{ref}}{N_i} \quad (4.7)$$

We define the average frequency error as follows:

$$\Delta F_{avg,i} = \frac{\sum_{n=1}^i \Delta F_n}{i} \quad (4.8)$$

System simulations were performed with deterministic signal edges as follows:

1. Set initial delay between the signal and clock edges (range: from 0 to $1/F_{ref}$)
2. For each i-th signal cycle determine and plot ΔF_i and $\Delta F_{avg,i}$
3. Repeat steps 1 and 2 for different initial phase

The averaging over 4 cycles is performed to achieve the required accuracy. The average frequency error for a deterministic input signal reduces at every iteration. The speed of error fading depends on signal and reference frequency ratios. When the input signal frequency is an integer multiple of the reference clock frequency, the error remains constant. In real application the sensor signal as well as the reference clock will always contain some jitter resulting in non-monotonic average error fading. After some averaging cycles the error will not decrease any further. For the highest input signal frequency of 4 kHz, the system simulation proves that specified sub-1 Hz frequency error can be achieved after 15 averaging cycles iterations. The error fading can also be observed when the signal value is not an integer multiple of the reference clock frequency. The system averaged frequency error simulation results for deterministic input signal edges are presented in Figure 4.43.

The system averaged frequency error simulation results when jitter with uniform distribution between ± 25 ns was added to the input signal edges are presented in Figure 4.44.

4.9.3 Circuit Design and Implementation

Present section will describe the details of the frequency signal conditioning circuit design. The top level circuit schematic is presented in Figure 4.45.

4.9.3.1 Input circuit

The sensor signal is applied to the ASIC via off-chip series resistors R_1 and R_2 located in the module, as shown in Figure 4.46. The half-wave rectification

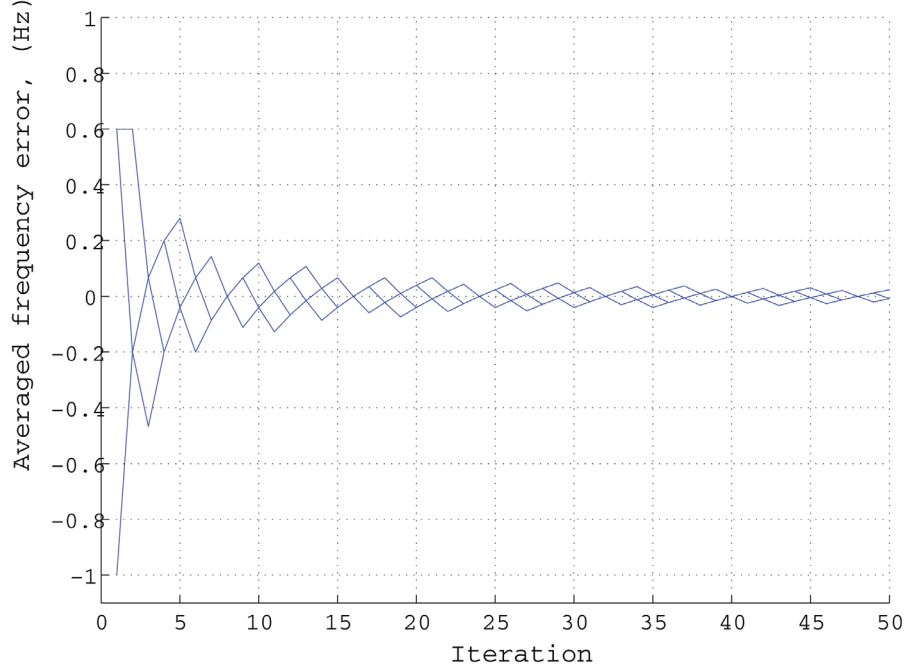


Figure 4.43 System averaged frequency error simulation results for a maximum input frequency $F_{sig} = 3999$ Hz and a reference clock frequency $F_{ref} = 10$ MHz.

and pulse detection is performed afterwards. The differential sensor signal is applied to two input circuits: one performing the signal reception and transformation for further processing while the other one being a dummy load for the sensor signal. Two $2.5\text{ k}\Omega$ resistors R_5 and R_6 at the input provide differential $5\text{ k}\Omega$ impedance required for proper sensor loading. Given the large input voltage amplitudes, resistors R_5 and R_6 are chosen to be high-power surface-mounted device (SMD) components specified for high temperature operation. The pn junction diodes, D_1 and D_2 , clamp the negative voltage, while positive voltage is converted to current and voltage by means of MOS diodes M_1 , M_2 and M_3 . Such a configuration of the input circuitry allows for the handling of low-amplitude signals (below 2 V or 4 V_{pp}) using the voltage processing chain, and large-amplitude signals (from 2 V up to 50 V) using the current conversion and detection circuit. The simulated MOS diode current and voltage outputs for multiple temperatures are presented in Figure 4.47. The border between the voltage-to-voltage and voltage-to-current processing lies between 1.5 V and 2 V , for different temperatures. Because of

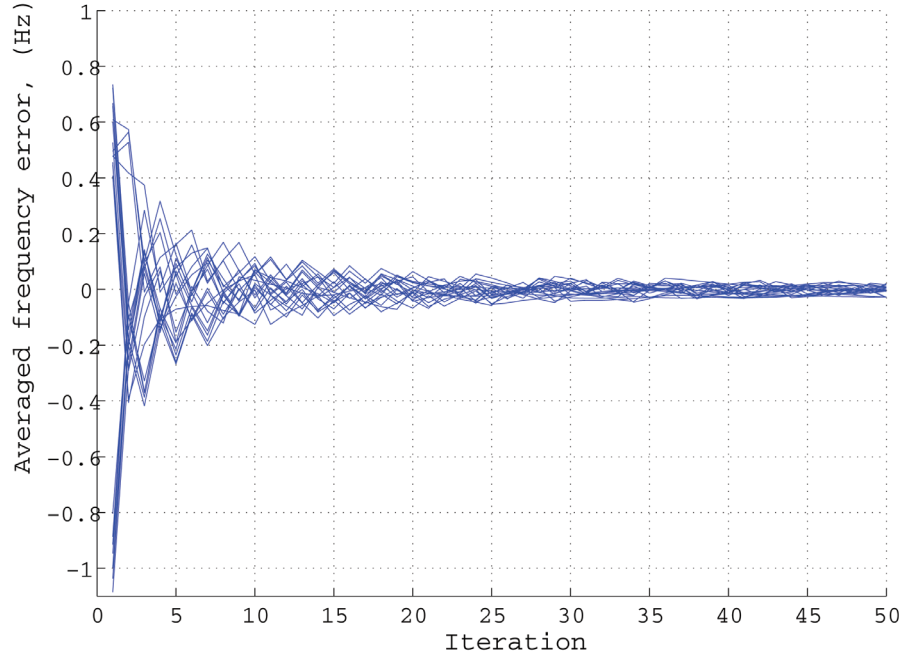


Figure 4.44 System averaged frequency error simulation results with added uniformly distributed jitter between ± 25 ns for a maximum input frequency $F_{sig} = 3999$ Hz and a reference clock frequency $F_{ref} = 10$ MHz.

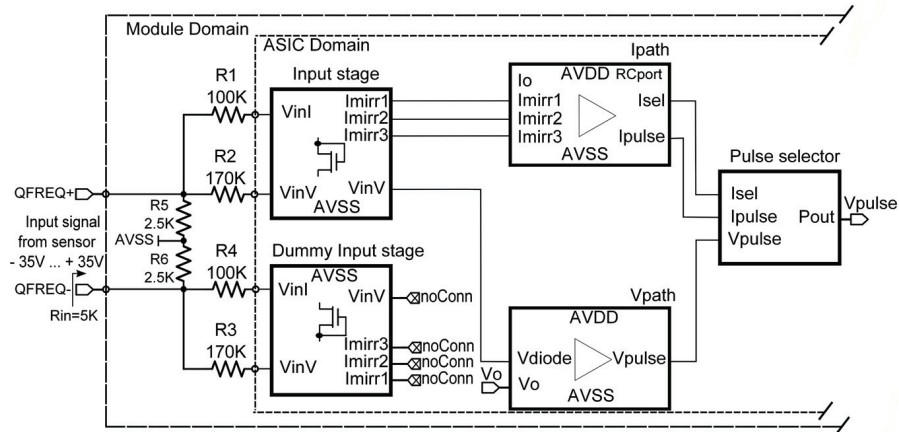


Figure 4.45 Top level circuit schematic of the signal conditioning unit processing the high voltage frequency signal.

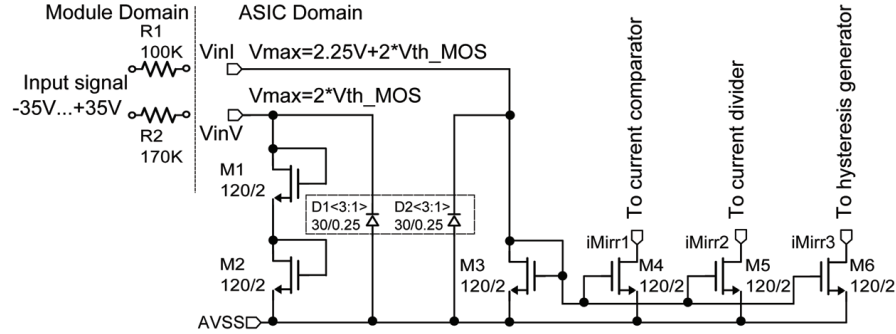


Figure 4.46 Input stage circuit schematic. Diodes D1, D2 are providing the current path for negative input voltage.

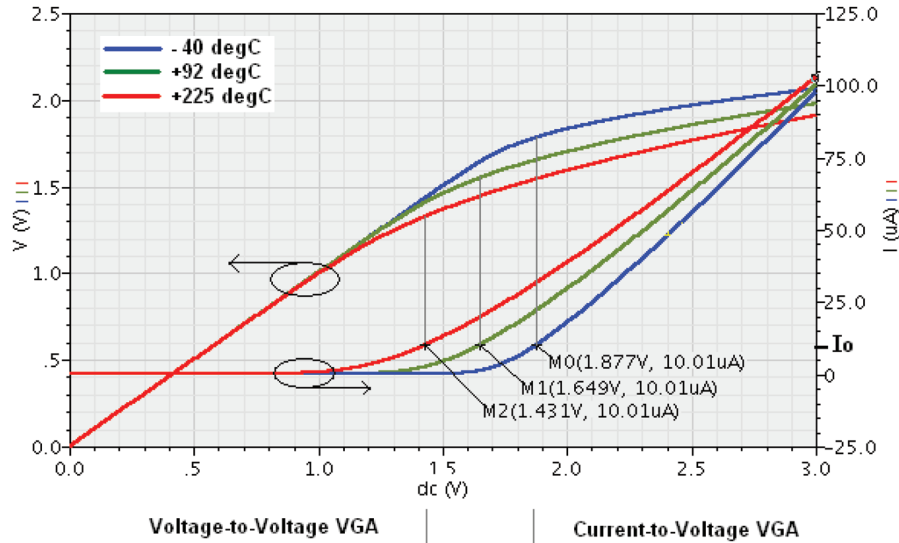


Figure 4.47 Simulated MOS diode current and voltage outputs over input signal for multiple temperatures.

the resistor-diode network, the voltage appearing at the ASIC is always within the supply voltage of the chip (5 V), therefore it is possible to utilize proper ESD protection at all pads.

The pulse detection principle based on peak current or voltage, and variable threshold is presented in Figure 4.48. The minimum peak value is set to prevent false triggering caused by noise. The peak value of the pulses is detected at

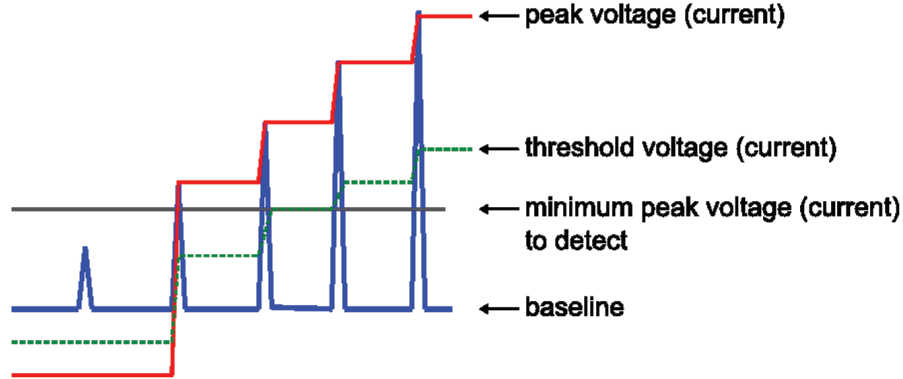


Figure 4.48 Pulse detection principle based on peak current (voltage) and variable threshold.

each cycle. The threshold value is generated from the peak value by dividing it by 2. Once a pulse overshoots the threshold, a digital output pulse is generated. For better noise immunity, the overshoot event is detected by a Schmitt trigger with the hysteresis window positioned around the threshold. The window opening is approximately 10% of the voltage range free of noise and amplitude variations.

The robustness of the signal conditioning unit against ESD event is considered for two handling cases: an electrostatic discharge directly at the ASIC inputs (event occurring during module assembly) and a discharge at the module input. High-ohmic off-chip resistors in series to ASIC inputs and 2.5 k Ω shunt load resistors protect the front-end circuitry from high currents, thus making ESD protection of the complete module very efficient. The Human body model (HBM) includes a 150 pF capacitance charged to ± 2 kV and a series 1.5 k Ω resistance [15]. When an ESD event according to HBM occurs at the module input (either differentially or between one input and ground), the R_5 and R_6 high power resistors divide the ± 2 kV voltage. The divided voltage is further applied to the ASIC inputs via resistors R_1 and R_2 . The MOS and pn diodes of the input circuit clamp the voltage at chip inputs keeping it within ± 5 V. Because of R_1 and R_2 the ESD current flowing into the ASIC does not exceed 20 mA, which complies with current limits specified for the X-FAB XI10 devices. Similarly, the ESD stress according to machine model (MM), 200 V charged capacitance discharging via a 0.5 μH inductance) does not cause any damage to the chip due to high-ohmic series resistors R_1 and R_2 and a diode-based input circuitry. The ASIC is less ESD immune against the event directly at chip inputs. The input MOS and pn diodes provide the

first-order protection. The possible overstress or damage may occur due to an excessive voltage or current during an ESD event. According to circuit simulations, the ASIC may directly withstand a stress up to 500 V HBM or up to 100 V MM. The robustness of ASIC inputs against ESD may be improved by placing dedicated protection structures at the inputs which on one hand are able to clamp large voltages/currents and on the other hand are generating low leakage currents at high operating temperatures, without distorting the input signal.

4.9.3.2 Current detect path

The circuit diagram of the current path including the current peak detector is presented in Figure 4.49. The input current is applied to the peak detector formed by the current comparator M_8 - R_1 , off-chip hold capacitor C_{ext} and the charge pump M_{12} - $OP1$. The current comparator generates the voltage V_{cmp} proportional to the difference between the applied input current and saturation current of M_8 . The sensitivity of the current comparator depends on the output impedance of M_8 and the impedance of the input current source r_s . A high sensitivity implies a high value of r_{ds8}/r_s . When the input current is higher than the peak current, V_{cmp} will be lower than V_{gs} , and M_{12} will pump current into C_{ext} to equalize the currents. When the input current is lower than the peak current, V_{cmp} will be higher than V_{gs} and the voltage at C_{ext} will not change. Because of this, the charge current for the hold capacitor C_{ext} is decoupled from the input current. This provides large time constants and a fast charge time while having a relatively low input current. The peak current of M_{12} can be several orders of magnitude larger than the input current. $OP1$ is the driver for M_{12} . In this way, the current peak detector is capable of detecting current pulses with sharp edges and low duty cycles. Threshold currents generated by M_9 and M_{10} form the hysteresis for the Schmitt trigger $TS1$, which detects the overshoot of the threshold by the input current pulse. Transistors M_5 , M_6 , and M_7 set the minimum peak current to be detected. Once the input current pulses exceed the minimum peak current value the output I_{sel} goes high indicating that the current sensing path is active. More details about I_{sel} are provided in Section 4.9.3.4. $OP1$ is a standard operational transconductance amplifier (OTA) [16] with a 2–4 V input common mode voltage range and a gain of 33 dB. The current sensing path was designed for a maximum value of the mirror currents I_{Mirr1} , I_{Mirr2} , I_{Mirr3} of 1 mA, 500 μ A and 550 μ A, respectively. Resistors R_1 – R_4 are reducing the sensitivity to noise voltage at the external RC port, they are limiting the bandwidth of the feedback

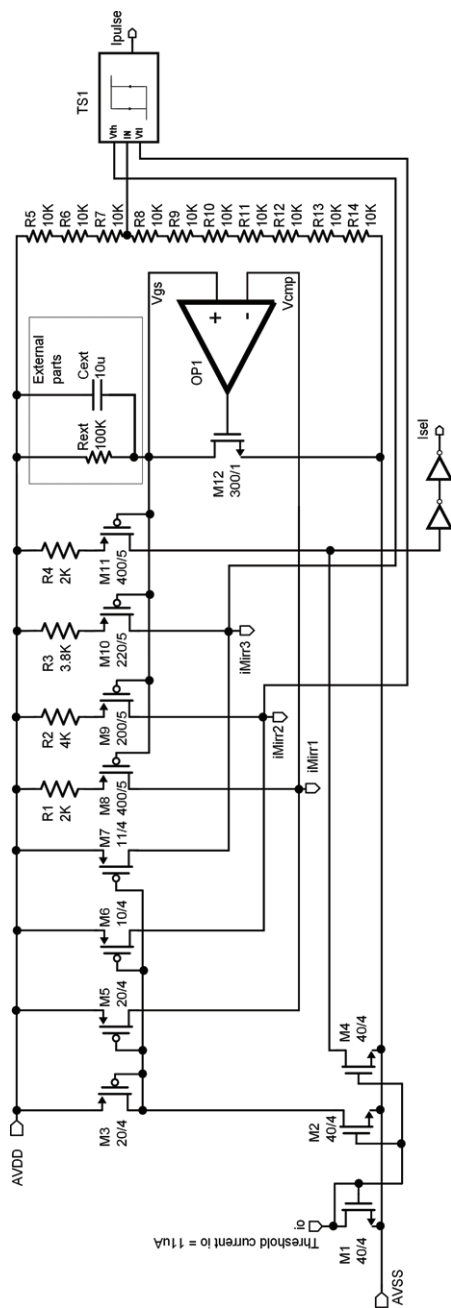


Figure 4.49 Circuit schematic and device sizes of the current sensing path.

circuit and they are increasing the voltage drop at the external R_{ext} , C_{ext} port for large DC currents. Their minimum value is defined by $R = 2V/I_{max} = 2\text{ k}\Omega$. The threshold current i_o , the mirror currents I_{Mirr1} , I_{Mirr2} , I_{Mirr3} and the bias currents of $OP1$ and $TS1$ in Figure 4.49 are generated by the bias block presented in [1]. The impact over pulse generation due to temperature and process variation of i_o , I_{Mirr1} , I_{Mirr2} and I_{Mirr3} is minimized by the high gain of the negative feedback network formed by $OP1$, M_{12} and (R_{ext}, C_{ext}) .

4.9.3.3 Voltage path

At low input voltages the current sensing path is disabled and detection is performed by the voltage sensing path. The circuit diagram of the voltage path is presented in Figure 4.50. The voltage peak detector is based on the charge pump $OP1$ - M_{12} and external hold capacitor C_{ext} . The voltage peak is detected only if the input signal overshoots the minimum voltage to be detected. The input signal is applied at V_{diode} to the PMOS voltage follower M_9 - M_8 . At the input of another voltage follower M_7 - M_6 , the minimum voltage to be detected of 0.2 V is applied. M_5 - M_4 sets the baseline voltage which is used to generate the threshold level by finding the average between the baseline V_{bl} and peak V_{peak} voltages. OpAmps $OP2$, $OP3$ and the resistive divider $R_1 \dots R_{10}$ implement this operation. Therefore, $OP2$ and $OP3$ have been designed as NMOS input class-AB output stage opamps, with a gain of 60 dB and an offset voltage of 10 mV. The output digital pulse is provided by the Schmitt trigger $TS1$. The hysteresis window opening is defined by the voltage drop on R_{10} and remains constant over the -40°C to 225°C temperature range. The schematic of the Schmitt trigger is presented in Figure 4.51. It is being used in both voltage and current detect paths and is implemented using two differential amplifiers and a RS-flip-flop. V_{tl} and V_{th} are setting the hysteresis levels for the device. When the input voltage overshoots the lower or upper thresholds, the RS-flip-flop is set to High or Low state by the respective amplifier. The advantage of the used circuit is independent of hysteresis window opening on temperature and temperature-independent current consumption defined solely by the biasing currents for differential amplifiers. The threshold voltages V_{tl} and V_{th} are dynamically changing with the amplitude of the input signal, as implemented in both current and voltage sensing blocks. While the voltage drop of D_1 - D_3 *pn*-diodes is 0.3 to 0.4 V smaller than the voltage drop on a MOS connected diode, the diode voltage drop dependence on temperature matches the minimum input voltage requirements of the $OP1$ differential pair

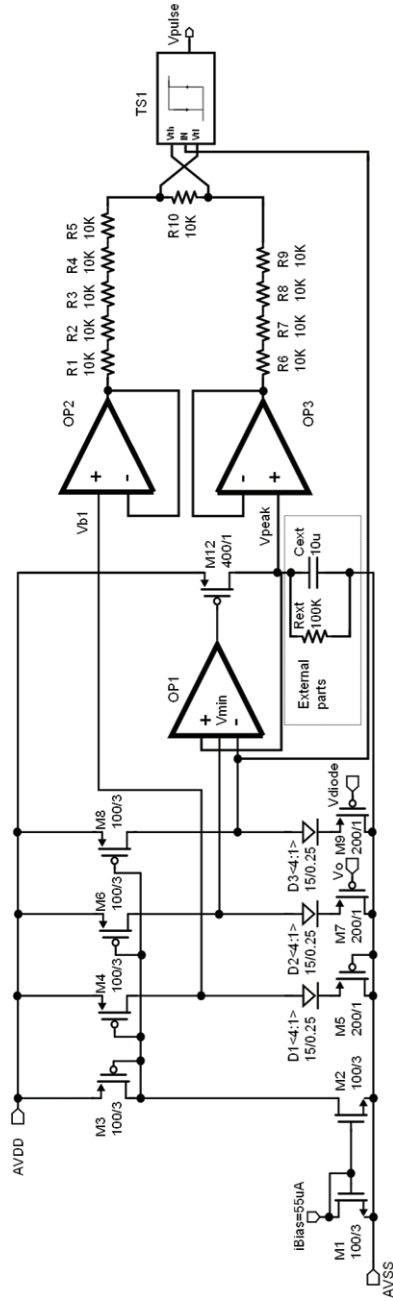


Figure 4.50 Circuit schematic, device sizes and bias current of the voltage sensing path.

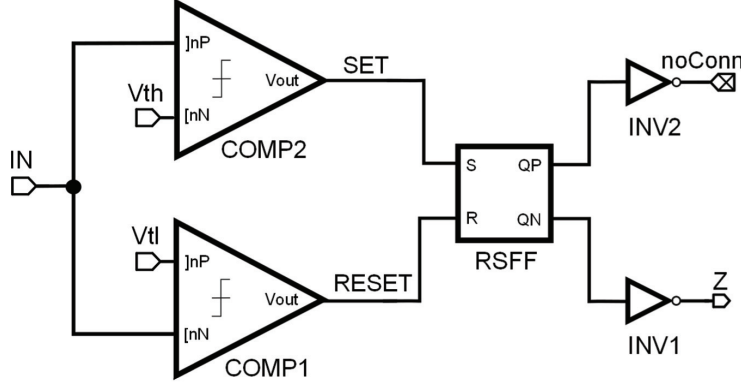


Figure 4.51 Circuit schematic of Schmitt Trigger.

to keep its current source in saturation. The bias current i_{Bias} of the voltage sensing path and the bias currents of $OP1$, $OP2$, $OP3$ and $TS1$ in Figure 4.50 are generated by the bias block presented in [1]. The impact over pulse generation due to temperature and process variation of i_{Bias} is minimized by the gain of the negative feedback network formed by $OP1$, M_{12} and (R_{ext}, C_{ext}) .

4.9.3.4 Pulse selector

The pulse selector presented in Figure 4.52 represents the interface between the voltage/current path and the following digital pulse counter. It validates either the output signal from the voltage detection path in Figure 4.49 or the current detection path 13 and send it further to the pulse counter. Based on the incoming pulses, the pulse counter block measures the frequency of the input sensor signal. The pulse counter was implemented together with the

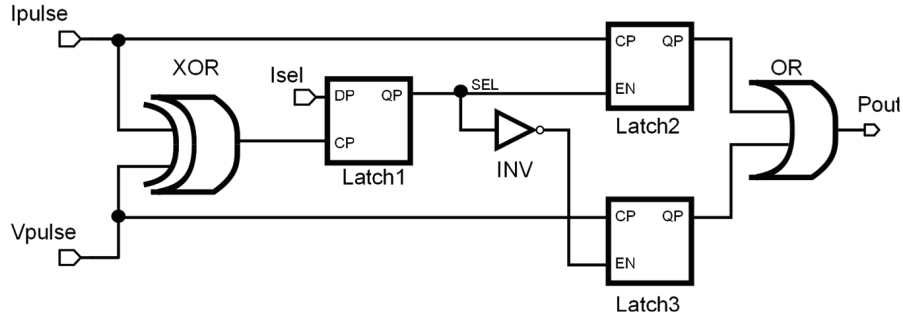


Figure 4.52 Pulse selector schematic.

ARINC429 transmitter in the digital flow, and is beyond the scope of this section.

The I_{sel} input indicates which one of the signal paths will be chosen. Two latched gated clock cells *Latch2* and *Latch3*, [17] are bypassing either I_{pulse} or V_{pulse} depending on the selection state. The change of selection state in-between the rising edges of I_{pulse} or V_{pulse} , namely t_1 and t_2 , is presented in Figure 4.53. If selection signal I_{sel} goes from low to high during t_1 neither I_{pulse} or V_{pulse} can generate the pulse at P_{out} . A no-triggering-error at the output P_{out} when both signal paths are active ($I_{pulse} = V_{pulse}$) is prevented by *XOR* and *Latch1* latching the I_{sel} control signal. In [3], the simulation results of an applied 4 kHz input signal and the detected pulses at the output with a width of 14 μs are presented.

4.9.4 Experimental Results

As mentioned in Section 4.9.2, the design principle of the HIGHTECS module was based on a custom SOI ASIC being used for the signal conditioning and signal processing from the range of sensors (i.e. temperature, strain gauges, frequency), multiplexing, analogue to digital conversion and transmission of data through an ARINC 429 databus. The HIGHTECS module helps reducing the weight of the helicopter engine by at least several kilograms [18]. The HIGHTECS ASIC was then integrated with voltage regulators, resistors and capacitors onto a ceramic hybrid circuit. The ceramic hybrid circuit was assembled in a hermetic Kovar package and hermetically sealed in an inert gas atmosphere. The Kovar package was then mounted into a stainless steel enclosure, as shown in Figure 4.54. In addition to the hybrid circuit, a high temperature printed circuit board (PCB) containing the high power SMD

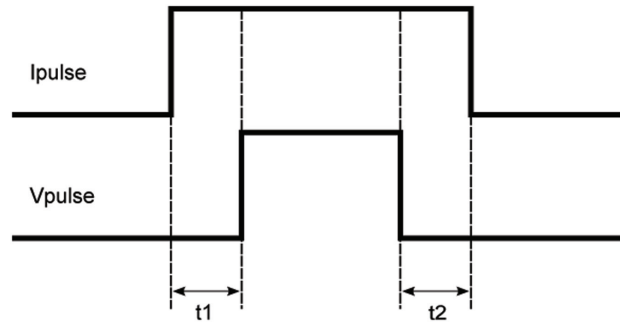


Figure 4.53 Pulse timing diagram.

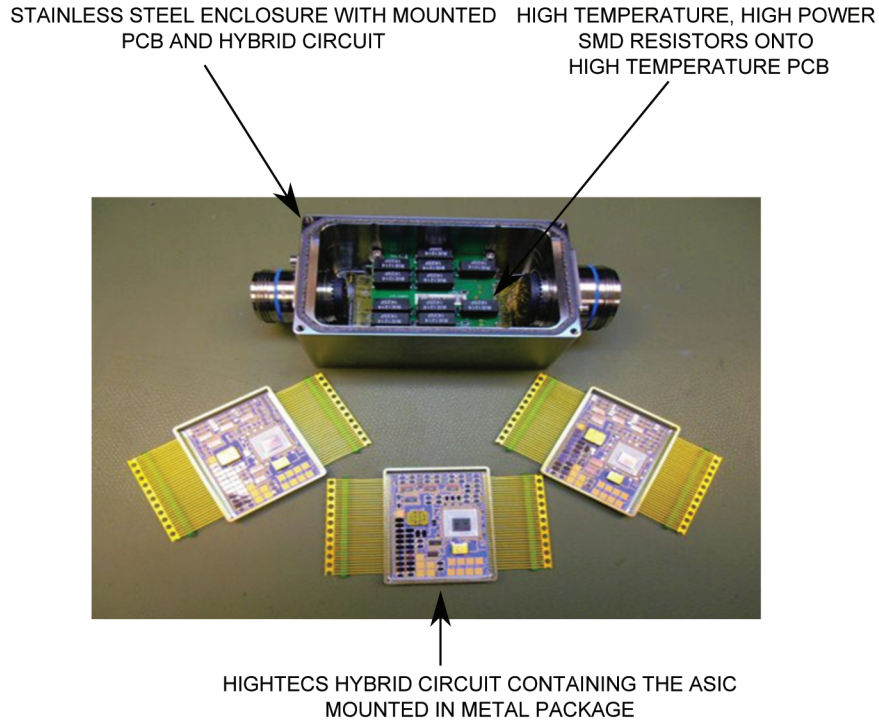


Figure 4.54 Stainless steel enclosure with mounted PCB and hybrid circuit including the HIGHTECS ASIC.

resistors for the frequency signal conditioning unit in Section 4.9.3.1 was designed and manufactured. This board was also mounted in the HIGHTECS module. The connections between the leads on the metal package, connection pads on the PCB and the connectors in the stainless steel enclosure were made with polyimide insulated copper wire. Several measurement results of the HIGHTECS hybrid have been published in [19].

In order to minimize the high temperature adverse effects such as material decomposition or phase change, increased stress due to coefficient of thermal expansion mismatches and leakage, the HIGHTECS ASIC was assembled in a 181-pin high temperature co-fired ceramic (HTCC) package and mounted onto a custom high temperature polyimide printed circuit board (PCB) to enable testing up to 235°C. The measurement results of the packaged HIGHTECS ASIC are reported below. The high temperature evaluation PCB is presented in Figure 4.55.

The proposed signal conditioning unit was fabricated in the 1 μm X-FAB SOI CMOS process. Figure 4.56 shows the layout of the frequency signal

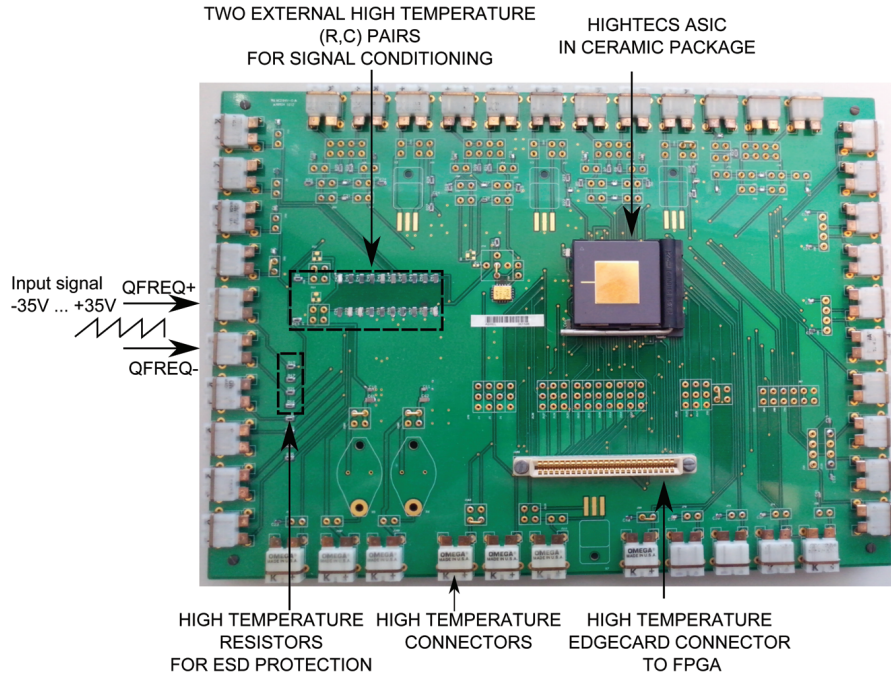


Figure 4.55 Photograph of the customized high temperature evaluation board used during HIGHTECS ASIC characterization measurements.

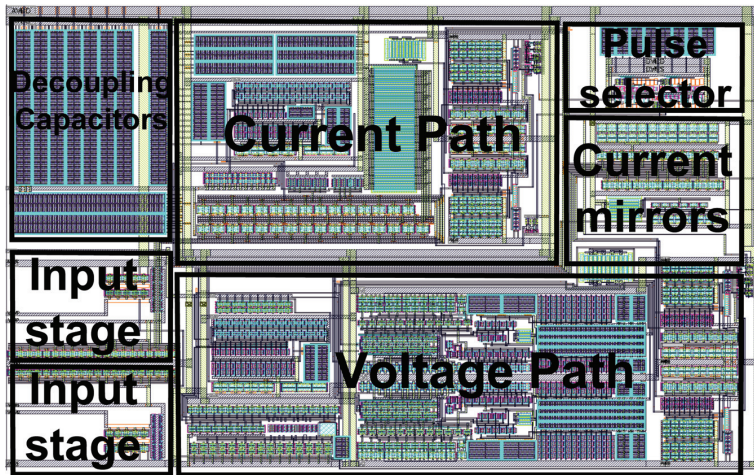


Figure 4.56 Layout of the frequency signal conditioning unit [1 mm × 1.5 mm] integrated onto the fabricated HIGHTECS ASIC.

conditioning unit included in the fabricated HIGHTECS ASIC. All devices were layouted as interdigitated devices to minimize the impact of thermal gradients. Figure 4.57 shows the micrograph of the HIGHTECS ASIC fabricated in the X-FAB XI10 SOI process [1]. The active area of the frequency signal conditioning unit, excluding the bonding pads and I/O drivers, is approximately 1.5 mm^2 . The system level test platform to measure the ARINC words from HIGHTECS ASIC are shown in Figure 4.58. The core circuit is powered by a 5 V analog and digital supply with separate grounds. For further noise reduction, decoupling high temperature capacitors are placed between power supply and grounds in the unused chip area. A software procedure to read the ARINC word via ChipScope was written in VHDL. This corresponds to the JTAG to USB bus in Figure 4.58. A digital receiver able to read the digital ARINC 429 output of the ASIC has been designed and implemented on a Xilinx XC3S500E FPGA (Spartan3E family) placed on a GODIL programming board. The GODIL board is providing a 49.152 MHz reference signal which is divided internally by 4 to generate a clock frequency of 12.288 MHz for the digital processor pulse counters. While the clock frequency of 12.288 MHz is higher than the specified value of 10 MHz in Section 4.9.2.2, it has the advantage that it is readily available on the test platform.

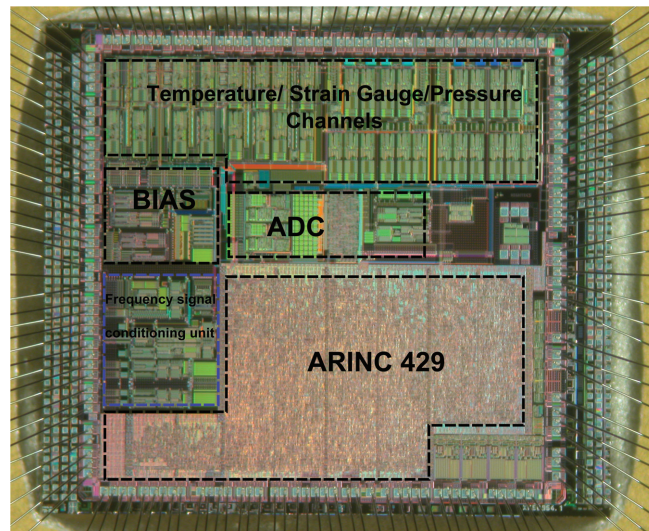


Figure 4.57 Micrograph of the bonded HIGHTECS ASIC fabricated in the X-FAB XI10 SOI process. The frequency signal conditioning unit is positioned on the left side the ASIC (in blue).

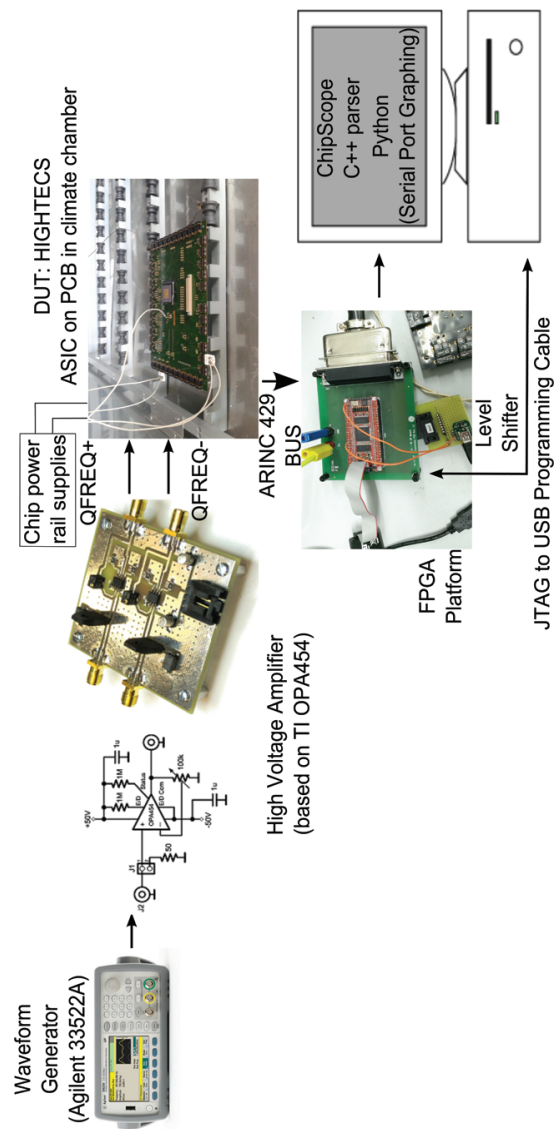


Figure 4.58 Block diagram of the HIGHTECS ASIC hardware & software test platform.

4.9.4.1 High voltage amplifier

The input signal was generated using a dual-channel waveform generator followed by a high voltage amplifier. An Agilent 33522A waveform generators provides a ± 5 V peak voltage levels. Therefore, an additional high voltage amplifier is required to generate the $V_{in} = 70 V_{pp}$ input signal. During testing, a sawtooth wave with $70 V_{pp}$ and 0 V offset was applied at the input of the frequency signal conditioning unit. The output data was read in from the ARINC data bus of HIGHTECS ASIC [1, 3]. The high voltage amplifier is based on the TI OP454 operational amplifier with supply voltage of up to ± 50 V. It operates only at room temperature and is connected through a high temperature cable assembly to the evaluation board.

4.9.4.2 Measurement results

The accuracy of frequency measurements directly depends on the accuracy of a reference generator, which is not a part of the HIGHTECS ASIC. The linearity of frequency measurements, however, is determined to most extent by the performance of signal conditioning and digital counting circuitry and is used as a measure for quantifying the performance of the HIGHTECS ASIC. Ideally, the linearity of frequency readings should be $R^2 = 1$. We specify the maximum allowed deviation of the measured output frequency from the linear trendline to be 1 Hz. This measure is independent of the absolute frequency of a reference clock generator and shows only the robustness of the HIGHTECS ASIC against temperature variation. Among the potential causes for linearity degradation in the presented unit are noise in the front-end circuitry, thresholds deviation over temperature, failures in the digital counters caused by temperature change etc.

The digital processor following the HIGHTECS ADC is performing the pulse counting for the ARINC 429 serial transmission. The processor's counters measure two periods t and t' of a sawtooth input signal which are the times between the sensor signal pulses: t is the time between loaded phonic wheel pulse and unloaded phonic wheel pulse; t' is the time between unloaded phonic wheel and loaded phonic wheel pulse. There are two sensor signal pulses for each cycle of the engine. The periods $t + t'$ are averaged over 4 cycles to improve the measurement accuracy and reduce the effects of noise. An error flag is set if the input frequency is greater than 4 kHz. The t and t' timers are 20 bit counters clocked at 12.288 MHz which are saturating when the maximum count is reached. The digital pulses coming out of the frequency signal conditioning unit are obtained by reading out the ARINC 429 serial bus

interface. The frequency of the input signal was swept between 50 Hz to 4 kHz across the 25°C–235°C temperature range to measure if the pulse readings and linearity varied across temperature. Measurement results are indicating the linearity of the output pulse counting measurements was very high ($>0.01\%$) and did not vary over temperature. Measurement results at 25°C and 235°C are presented in Figures 4.59 and 4.60, respectively. The measurements were limited at 235°C due to the maximum temperature specification of the PCB mounted capacitors and of the polyimide material of the PCB.

There are virtually no differences between the measurement results at 25°C and those at the maximum temperature of 235°C, which shows the temperature stability of the design. Based on the measured R^2 linearity values, a maximum averaged frequency error of 0.3 Hz was calculated which is fulfilling the frequency error requirement Table 4.10 presents the specification versus measurement results.

The linearity values of the output pulses counting versus temperature are presented in Figure 4.61. Measurement results of several HIGHTECS ASICs are indicating same linearity values for the first past comma seven digits.

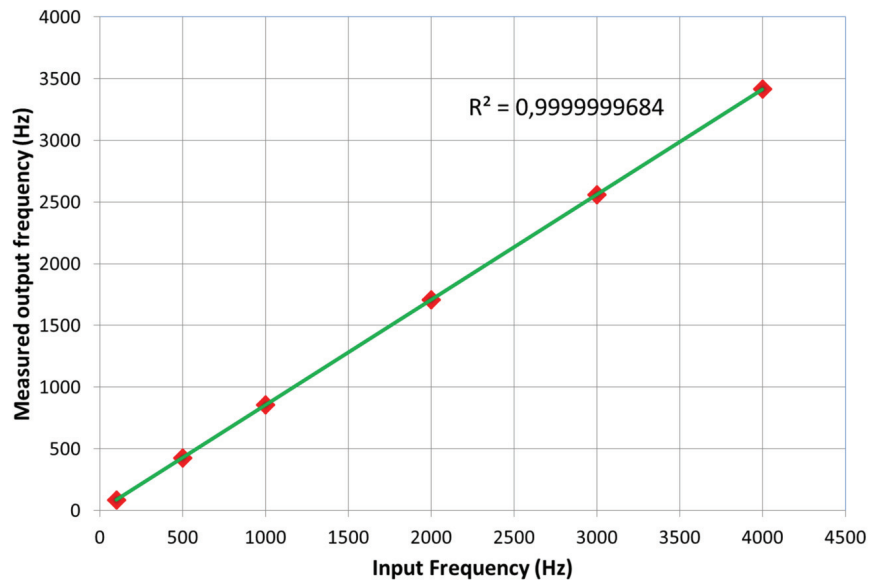


Figure 4.59 Measured output frequency (red dots) via ARINC and FPGA at 25°C shows a linearity value of $R^2 = 0.9999999684$ with a reference clock frequency of $F_{ref} = 12.288$ MHz.

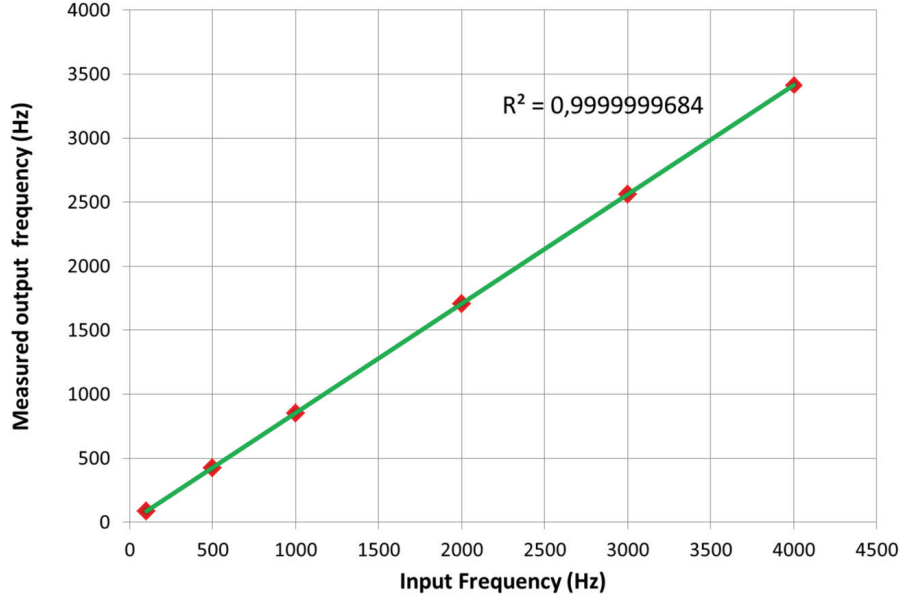


Figure 4.60 Measured output frequency (red dots) via ARINC and FPGA at 235°C shows a linearity value of $R^2 = 0,9999999684$ with a reference clock frequency of $F_{ref} = 12.288$ MHz.

Table 4.10 Specification versus measurement results

Parameter	Specification	Measurement	Units
Temperature	200	235	°C
F_{min}	50	50	Hz
F_{max}	4000	4000	Hz
V_{in}	70	70	V
$\Delta F_{avg,i}$	<1	<0.3	Hz
F_{ref}	10	12.288	MHz

The presented signal conditioning unit is a discrete-domain conditioning system which detects the frequency of a periodical input signal. The frequency detection is free of errors as the front-end circuitry is correctly detecting the rising/falling edges of the input signal using internally-generated threshold voltages. Even though the absolute values of threshold voltages/currents vary slightly with temperature, the temperature variations are low enough for the error-free detection of input signal edges, and thus frequency. The time jitter caused by temperature-dependent thresholds is well below the period of the $F_{ref} = 12.288$ MHz reference clock.

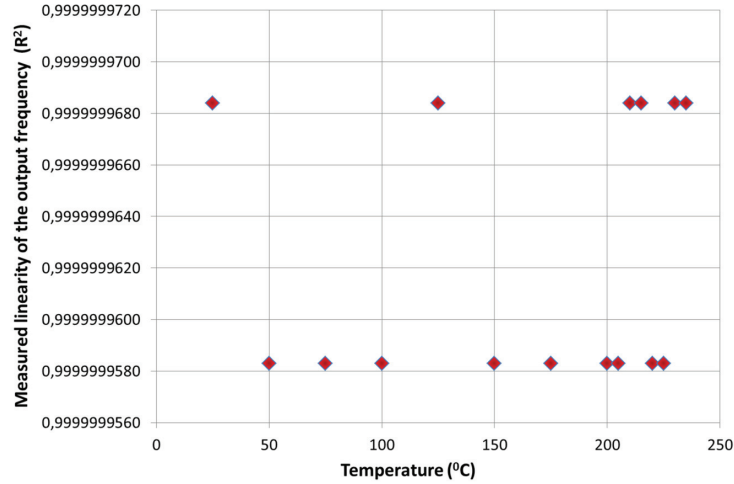


Figure 4.61 Measured linearity values (R^2) of the output frequency over the 25°C to 235°C temperature range are within specification limits. The reference clock frequency value is $F_{ref} = 12.288$ MHz.

References

- [1] L. Stoica, V. Solomko, T. Baumheinrich, R. D. Regno, R. Beigh, S. Riches, I. White, G. Rickard, and P. Williams, “Design of a high temperature signal conditioning ASIC for engine control systems – HIGHTECS,” in *Proc. IEEE International Symposium on Circuits and Systems*, Melbourne, Australia, May. 2014, pp. 2117–2120.
- [2] R. Hogervorst, “Design of a low-voltage low-power CMOS operational amplifier cells,” Ph.D. dissertation, Univ. of Delft, Delft, The Netherlands, Jun. 1996.
- [3] L. Stoica, V. Solomko, T. Baumheinrich, R. D. Regno, R. Beigh, I. White, G. Rickard, and P. Williams, “Design of a frequency signal conditioning unit applied to rotating systems in high temperature aero engine control,” in *Proc. IEEE International Symposium on Circuits and Systems*, Lisbon, Portugal, May. 2015, pp. 1154–1157.
- [4] D. Flandre, L. Demeus, V. Dessard, A. Viviani, B. Gentinne, and J. P. Eggermont, “Design and application of SOI CMOS OTAs for hightemperature environments,” in *Proc. IEEE 24th European Solid-State Circuit Conference*, The Hague, The Netherlands, Sep. 1998, pp. 404–407.
- [5] R. Hogervorst, J. Tero, R. Eschauzier, and J. Huijsing, “A compact power-efficient 3V CMOS rail-to-rail input/output operational amplifier for VLSI cell libraries,” *IEEE J. Solid-State Circuits*, vol. 29, pp. 1505–1513, Dec. 1994.

- [6] J. Huijsing, *Operational amplifiers*. Dordrecht, The Netherlands: Springer Science+Business Media B.V., 2011.
- [7] Y. Lam, and W. Ki, "CMOS bandgap references with self-biased symmetrically matched current-voltage mirror and extension of Sub-1-V design," *IEEE Trans. VLSI Sys.*, vol. 18, no. 6, pp. 857–865, June 2010.
- [8] L. Stoica; R. Ghandi; Cheng-Po Chen; E. Andarawis; V. Solomko; S. Riches, "A signal conditioning unit for high temperature applications, 2016 IEEE International Symposium on Circuits and Systems (ISCAS), Year: 2016, Pages: 2403–2406.
- [9] L. Stoica; V. Solomko; T. Baumheinrich; R. Del Regno; R. Beigh; G. Rickard; P. Williams; S. Riches, "A High Temperature Frequency Signal Conditioning Unit for Aeronautical Rotating Systems", *IEEE Transactions on Circuits and Systems I: Regular Papers* Year: 2016, Volume: 63, Issue: 5.
- [10] K. Koli and K. Halonen, "Low voltage mos-transistor-only precision current peak detector with signal independent discharge time constant," in *Proc. IEEE International Symposium on Circuits and Systems*, Hong Kong, PRC, Jun. 1997, pp. 1992–1995.
- [11] C. Mead, R. Lyon, and R. Sarpeshkar, "A low-power wide dynamic range analog VLSI cochlea," *Analog Integrated Circuits and Signal Processing*, vol. 16, pp. 245–274, Aug. 1998.
- [12] R. Sehgal, A. Singh, and W. Serdijn, "CMOS ultra low-power wavelet filter based sense amplifier for cardiac signal analysis," in *Proc. 19th Annual Workshop on Circuits, Systems and Signal Processing (ProRisc)*, Veldhoven, The Netherlands, Nov. 2008, pp. 260–266.
- [13] S. Zhak, M. Baker, and R. Sarpeshkar, "A low-power wide dynamic range envelope detector," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1750–1753, Oct. 2003.
- [14] ARINC429. (2015, Sep.) ARINC 429 Overview. [Online]. Available: <https://www.aim-online.com/pdf/OVIEW429.PDF>
- [15] M. Ker, J. Peng, and H. Jiang, "ESD test methods on integrated circuits: an overview," in *Proc. IEEE International Conference on Electronics Circuits and Systems*, Valetta, Malta, Sep. 2001, pp. 1011–1014.
- [16] R. Baker, *CMOS Circuit Design, Layout and Simulation*. Hoboken, New Jersey: John Wiley & Sons Inc., 2008.
- [17] J. Yuan and C. Svensson, "High-speed CMOS circuit technique," *IEEE J. Solid-State Circuits*, vol. 24, pp. 62–70, Feb. 1989.
- [18] J. Rigaud and L. Stoica, "Turbomeca TCON," Oct. 2015, Meeting Notes.
- [19] S. Riches, C. Warn, K. Cannon, G. Rickard, and L. Stoica, "Design and assembly of high temperature distributed aero-engine control system demonstrator," in *Proc. International Conference on High Temperature Electronics (HiTEC)*, Albuquerque, United States, May. 2014.